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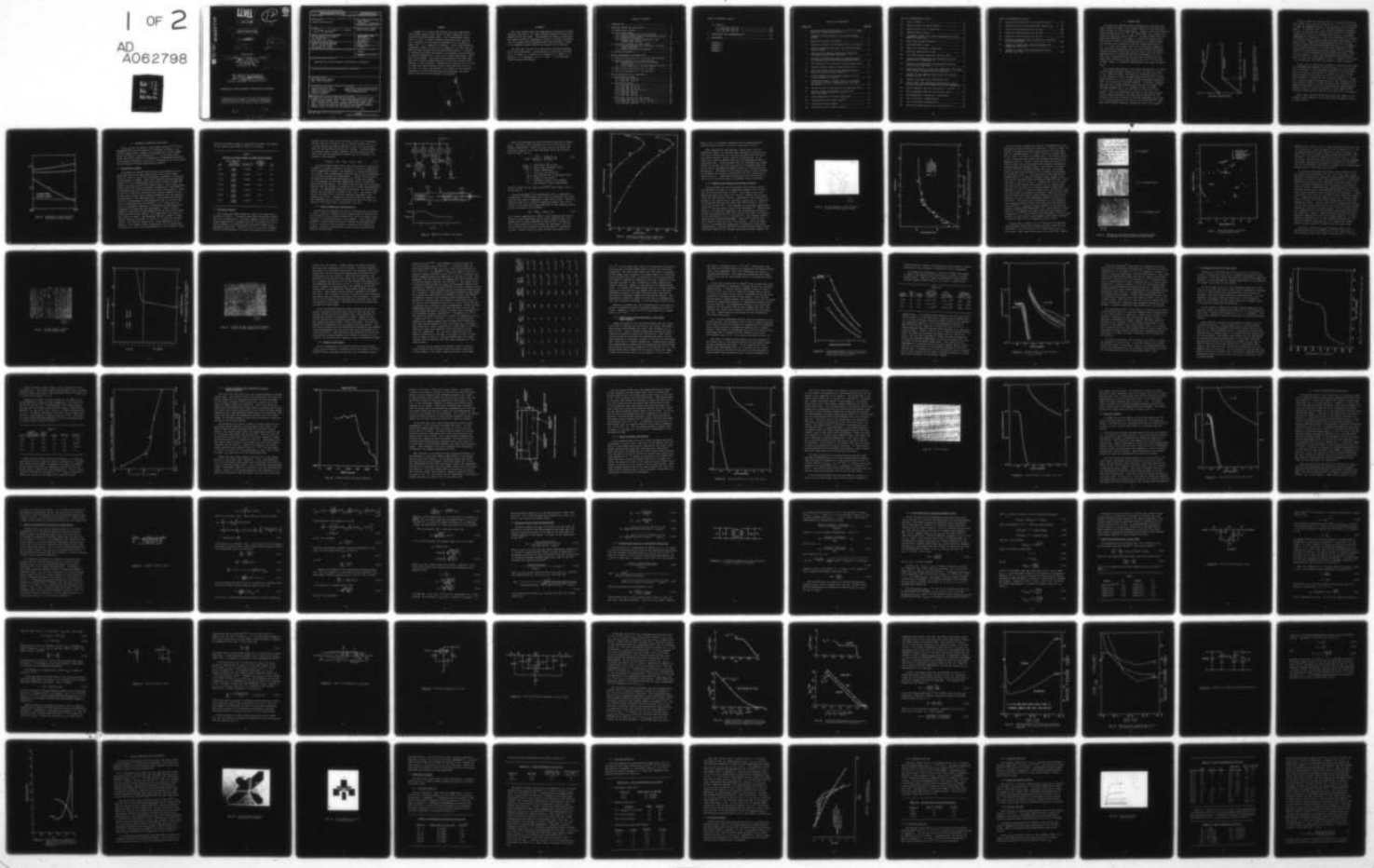

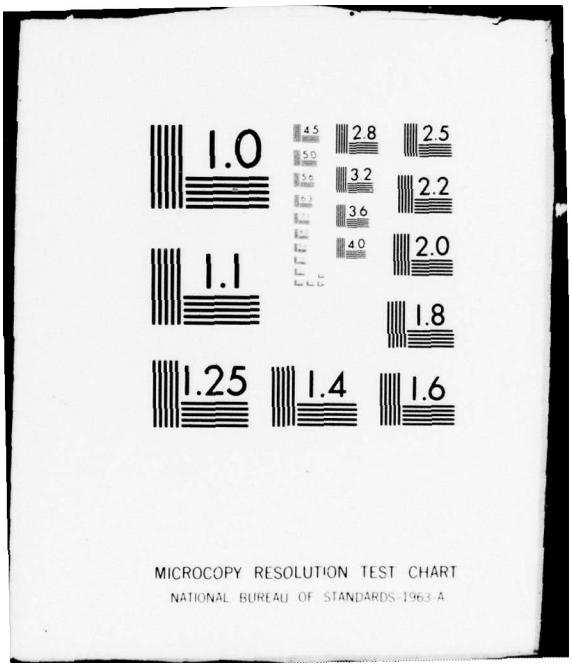
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(10) S. G. Bandy, S. B. Hyder, T. J. Boyle, C. K. Nishimoto

VARIAN ASSOCIATES, INC.
611 Hansen Way
Palo Alto, CA 94303

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A number of low-noise FET devices have been fabricated using InGaAs active layers grown on GaAs substrates with an intervening graded buffer layer. The In percentages range from 0 to 34%. In spite of velocity degradation at the active layer-buffer layer interface and the use of lower-doped channels, InGaAs is able to match the performance of GaAs.

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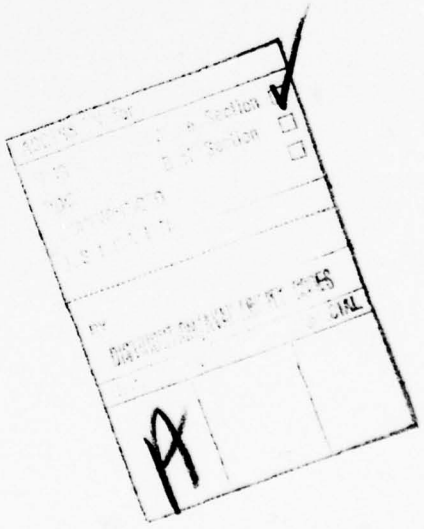
SUMMARY

A number of low-noise FET devices have been fabricated using InGaAs active layers grown on GaAs substrates with an intervening graded buffer layer. The In percentages range from 0 to 34%. A higher effective saturated drift velocity v_s is expected for this material because as In is added to GaAs, the Γ to L separation increases. Using three different techniques, about a factor of 1.5 increase in v_s over that for GaAs has been deduced from the FET characteristics. A method of velocity profiling the channel is presented, and the problem of velocity degradation at the active layer-buffer-layer interface is discussed. The noise figure minimum occurs near zero gate bias, further substantiating the notion of velocity degradation at the interface. Minimum noise figures of 2 to 2.5 dB at 8 GHz have been obtained with an associated gain of 12 to 14.5 dB. To realize the benefit of a higher v_s, the velocity degradation at the interface must be eliminated, and steps taken to alleviate this problem are discussed.



FOREWORD

The work reported here was supported by the Office of Naval Research, Washington, DC, under contract N00014-75-C-0125, and managed by Mr. Max Yoder. The program was aimed at developing the InGaAs materials technology in order to evaluate its potential for superior FET performance over that for GaAs in light of its expected higher effective saturated drift velocity.

The work was carried out in the Varian Corporate Research Solid State Laboratory. Contributions to this work were made by S. G. Bandy, T. J. Boyle, D. R. Decker, S. B. Hyder, R. D. Fairman, C. K. Nishimoto, and R. L. Bell. J. H. Dully provided technical assistance.

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1. INTRODUCTION

The important parameter which determines the limiting frequency response of FETs is the transit time which the electrons take to cross the active gate region. Figure 1 shows the velocity-field characteristic for 10^{17} cm^{-3} doped GaAs[1] and a simple two-piece fit typically used to model it. As gate lengths have progressively decreased in an effort to reduce the transit time, the electric fields in the channel exceed to a greater degree the threshold for intervalley transfer (approximately E_s in Fig. 1). Since the transit time is not large with respect to the intervalley scattering time, one must consider the actual electron dynamics rather than just the static velocity-field characteristic in estimating what FET performance will be.[2,3] This need is demonstrated by the fact that although the high field drift velocity for GaAs exceeds that for Si by only 10% at most, there is a dramatic improvement in the figure of merit f_{max}.[2]

The optimum FET material would allow the electrons to travel at the highest possible velocity in the Γ minimum (i.e. have a low Γ effective mass), and spend the longest possible time at high energies in the Γ minimum before transferring into the upper valleys (i.e. have a large intervalley energy separation and a low intervalley coupling constant). Although it appears that InP has a slightly higher peak velocity than GaAs,[4] the coupling constant for Γ to L transfer in GaAs is around 3×10^8 eV cm^{-1},[5] while that for InP is in the $5\text{-}14 \times 10^8$ range.[6] Since the scattering time goes as the inverse square of the coupling constant, the more rapid scattering of the electrons into the L valleys in InP will compensate the higher Γ to L energy separation (0.6 eV vs 0.38 eV for GaAs[5,6]) somewhat when velocity overshoot effects are taken into account.

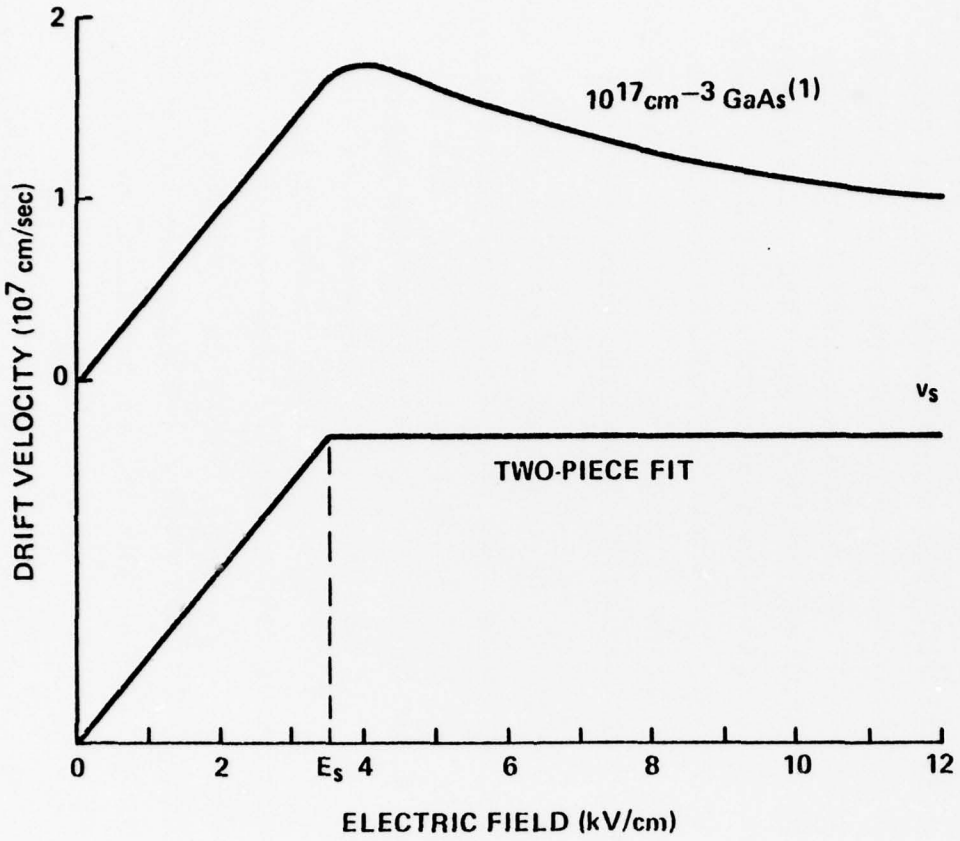


Figure 1. Velocity-field characteristic for $10^{17}cm^{-3}$ doped GaAs and a simple two-piece fit.

Figure 2 shows the position of the Γ, X, and L minima for the ternary $In_xGa_{1-x}As$ as a function of x.[7-10] As In is added to GaAs the bandgap decreases, thus decreasing the Γ effective mass.[11] In addition, the Γ to L energy separation increases so that the threshold for upper valley transfer is increased, assuming that the Γ to X coupling coefficient is relatively independent of composition. This will contribute to shortening the electron transit time through the active gate region, and should lead to improved FET performance over that for GaAs. Although InGaAs has been considered previously as a candidate for an optimum material,[12] an artificial constraint of the intervalley energy separation being larger than the bandgap led to its being considered less desirable than InAsP. GaAs, the best material to date for demonstrated FET performance, does not meet this requirement, and Fig. 2 suggests that InGaAs is an improvement over GaAs with respect to this criterion.

$In_xGa_{1-x}As$ also offers the advantage of differing from GaAs only incrementally depending upon the value of x, so at least for low values of x the processing technology for GaAs should also be suitable if not better for InGaAs (e.g. the reduced barrier height should reduce the contact resistance of the ohmic contacts). Except for the very high values of x, InGaAs has a barrier height advantage over InP. The technique of lattice matching InGaAs to a semi-insulating GaAs substrate by a graded region grown by VPE has been previously demonstrated,[13] enabling InGaAs to enjoy the benefits of the superior semi-insulating GaAs substrate quality over that of InP, for example.

These, then, are the motivating reasons why InGaAs is considered a good candidate for obtaining FET performance superior to that of GaAs.

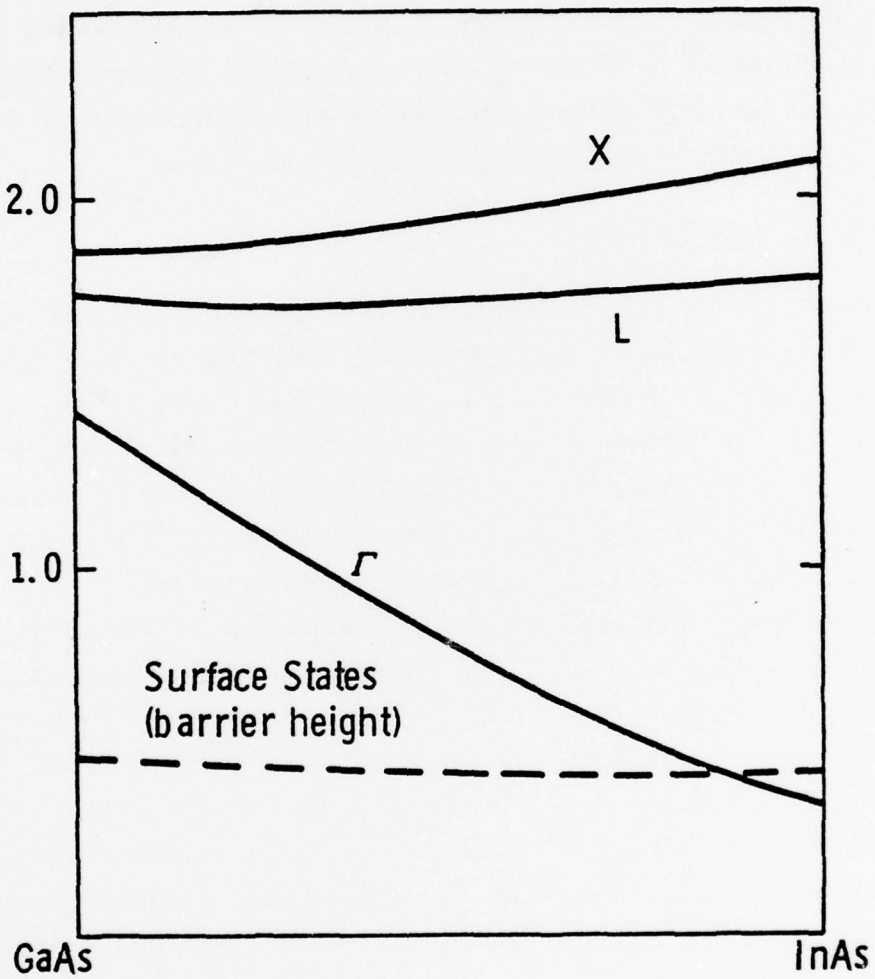


Fig. 2: Schematic of band edges for the InGaAs ternary system.

2. MATERIALS GROWTH AND EVALUATION

$In_xGa_{1-x}As$ can be grown by liquid phase epitaxy,[8,14,15] but homogeneous FET quality material is difficult to obtain, and uniform compositional grading is also difficult by this method. Growth by chemical vapor deposition,[16-18] on the other hand, lends itself more readily to preparation of homogeneous material of any desired composition and donor concentration by facilitating lattice matching through compositional grading.

2.1 Mixed Source System

To provide the needed graded buffer layer between the Cr-doped semi-insulating GaAs substrate and the active InGaAs epitaxial layer to avoid lattice-mismatch problems, a two-source source system is needed. While this system was being developed, layers of low In concentration were grown directly on GaAs substrates by using a mixed In-Ga source system. This simply involved using the $AsCl_3$,H_2 transport system used to grow GaAs[19-21] and substituting the Ga source with a mixed In-Ga source. Ratios of 24%/1.3%, 32%/1.8%, and 50%/2% are typical examples of the relationship between the In source percentage and the resulting In percentage in the deposited film. One problem with controlling the In percentage in the deposited films is the fact that the In is depleted from the source at 3 to 4 times the rate the Ga is depleted, resulting in decreasing In percentages for subsequent runs made from the same source. Table I gives a summary of the mobility data obtained for the thin layers grown using the mixed source system. For comparison, data from two GaAs films are shown. The bracketed mobility listed is "best typical" mobility obtained on thicker (> 0.5-micron) epitaxial layers. The mobility values are at least comparable if not better for the InGaAs layers, showing that for In percentages at least up to 2.5% the lattice-mismatch at the substrate inter-

face is not severe enough to significantly affect the quality of the overall layer when as thin as 0.3 micron.

TABLE I

MOBILITY OF LAYERS GROWN IN MIXED SOURCE SYSTEM

Run	Hall Mobility at 300°K (cm^2/V-sec)	N_D-N_A (cm^{-3})	Layer Thickness (μm)	%In
25-1	4640 (4700)	9.4e16	4.6	1.3
25-14	4106 (4600)	1.0e17	~ 0.6	2.0
25-15	3758 (4650)	9.6e16	0.3	2.0
25-16	4512 (4500)	1.2e17	~ 0.6	2.3
25-17	3889 (4600)	1.0e17	0.4	2.5
22-21	3348 (4600)	1.0e17	0.2	0
24-9	3293 (4500)	1.2e17	0.4	0

2.2 Two-Source System

The $In_xGa_{1-x}As$ growth system and reactor are shown schematically in Fig. 3. Electronic mass flow controllers control the flow of purified H_2. The $AsCl_3$ bubbler is kept at any desired temperature by a thermal bath and is connected to the In and Ga chambers; the $AsCl_3/H_2$ flow over each element being separately controlled. The flow line to In is also connected through valved bypasses to an etch line entering the reactor

chamber, and the flow can be diverted to this line if desired. The H_2S tank gas (310 ppm in H_2) is further diluted with H_2 in a mixing chamber and the diluted gas is fed into the reactor ahead of the substrate position for S doping. Chromium doping is achieved using a CrO_2Cl_2 bubbler, and the CrO_3/H_2 mixture enters the reactor between the sources and the substrate, according to the reaction

$$3CrO_2Cl_2 + 3H_2 \rightarrow CrO_3 \cdot Cr_2O_3 + 6HCl \quad . \qquad (2\text{-}1)$$

The monochloride vapors of Ga and In are mixed in the reactor by means of a baffle placed at the exit of the In/Ga chambers to ensure homogeneous mixing. The substrate is placed horizontally in a holder, and a thermocouple inserted into a well incorporated in the holder records the temperature. A quartz liner protects the reactor from monochlorides depositing in the cold region. All the glassware in the high temperature region is made from Spectrosil grade quartz. The reactor tube is held in a horizontal position and the furnace is rolled onto it to start the deposition process. An approximate temperature profile of the furnace when placed over the reactor is shown in Fig. 3(c). The source temperature was about 780°C, and the substrate temperature was usually about 720°C. Temperature variation over the length of the substrates was less than a degree/cm and about 5°C over the length of the source boats, which were 8 cm long.

2.2.1 Source Preparation and Saturation

Fifty grams of elemental In and Ga of minimum purity 99.9999% is used. Gallium is poured into the source boat as received but In is baked in a H_2 stream at about 900°C for 72 hr before transferring it to the source boat in the reactor. Use of $AsCl_3$ and elemental sources requires that the sources are saturated with As until a crust of InAs and GaAs is formed on the respective sources. Transport and epitaxial growth occurs only after the sources are saturated.

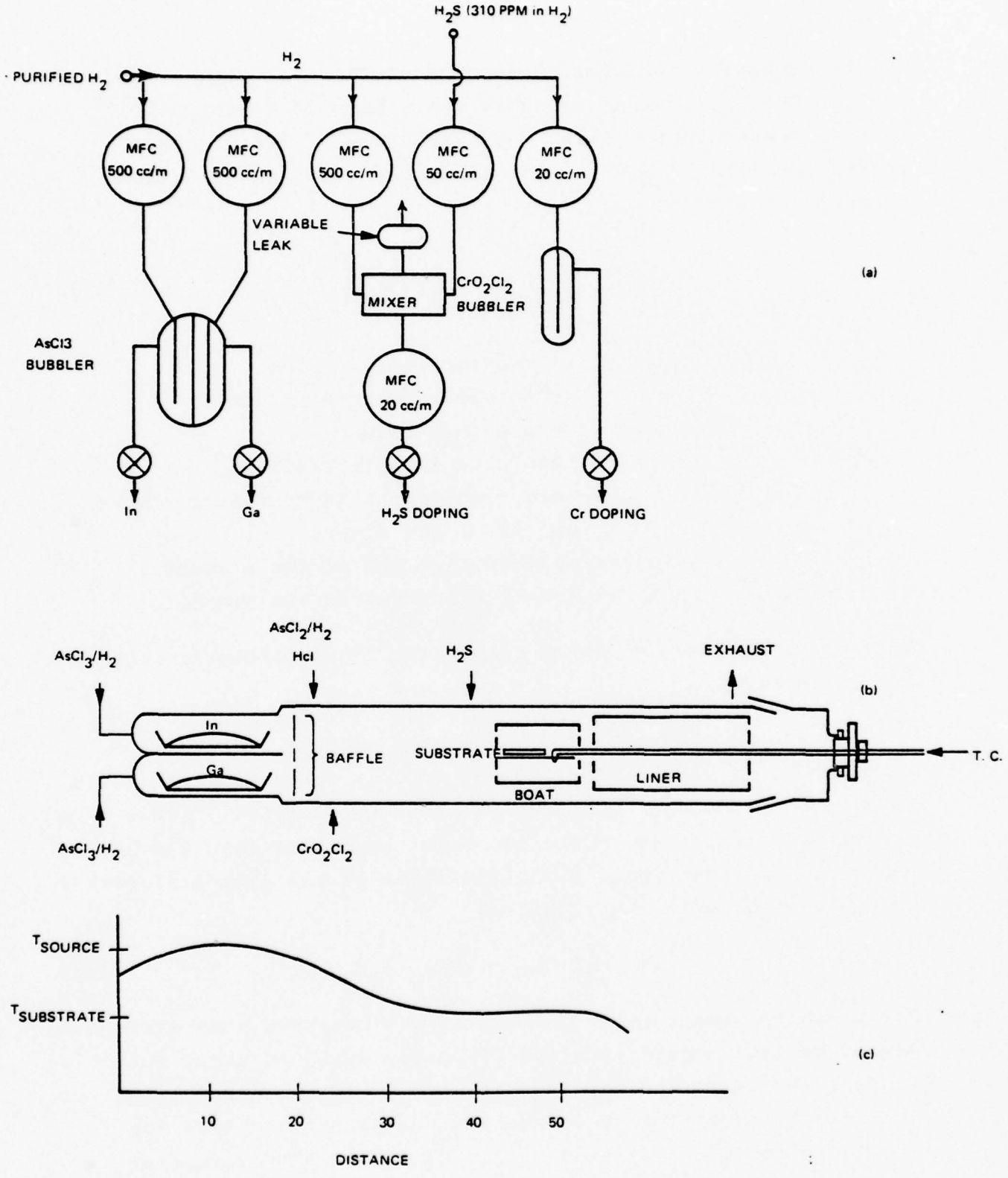


Fig. 3. Deposition reactor and system.

The source temperature during saturation was kept at about 770°C. The $AsCl_3$ vapor pressure was 9.15×10^{-3} atm at 20°C bubbler temperature. Using a H_2 flow rate of 300 cc/min the saturation time of 5.6 hr was calculated using the relation given by Shaw[21] for Ga,

$$t_{satu} = \frac{RT_1}{P_{AsCl_3} F_1} \cdot \left[\frac{X_{As}}{1-X_{As}}\right] \frac{W}{m \cdot w} \qquad (2\text{-}2)$$

t_{satu} = saturation time in min
P_{AsCl_3} = $AsCl_3$ vapor processes (atm)
T_1 = source temperature
F_1 = flow rate in liters/min
X_{As} = mole fraction As in saturated source
W = weight of the source
$m \cdot w$ = molecular weight of the element
R = gas constant 0.0821 atm/deg-mole

Arsenic solubility was taken from Hall's[22] data shown in Fig. 4 for Ga and In.

Ban and Ettenberg[23] have calculated that at a deposition temperature of 1000°K about 10% of InCl is converted into solid from the gas phase as compared to about 60% for GaCl. This also indicates that the In source is depleting faster than the Ga source in the same ratio since depletion of the elemental source occurs according to the relation,

$$2M_l + 2HCl_g \rightarrow 2MCl_g + H_2 \quad . \qquad (2\text{-}3)$$

For a source temperature of 780°C it was observed that after a series of test depositions the Ga source depleted about 20% whereas the In source depleted as much as 80%. Considering this faster depletion of In source, the saturation time for the In source was estimated by dividing Shaw's[21] expression by four. Indium saturation time was then calculated to be

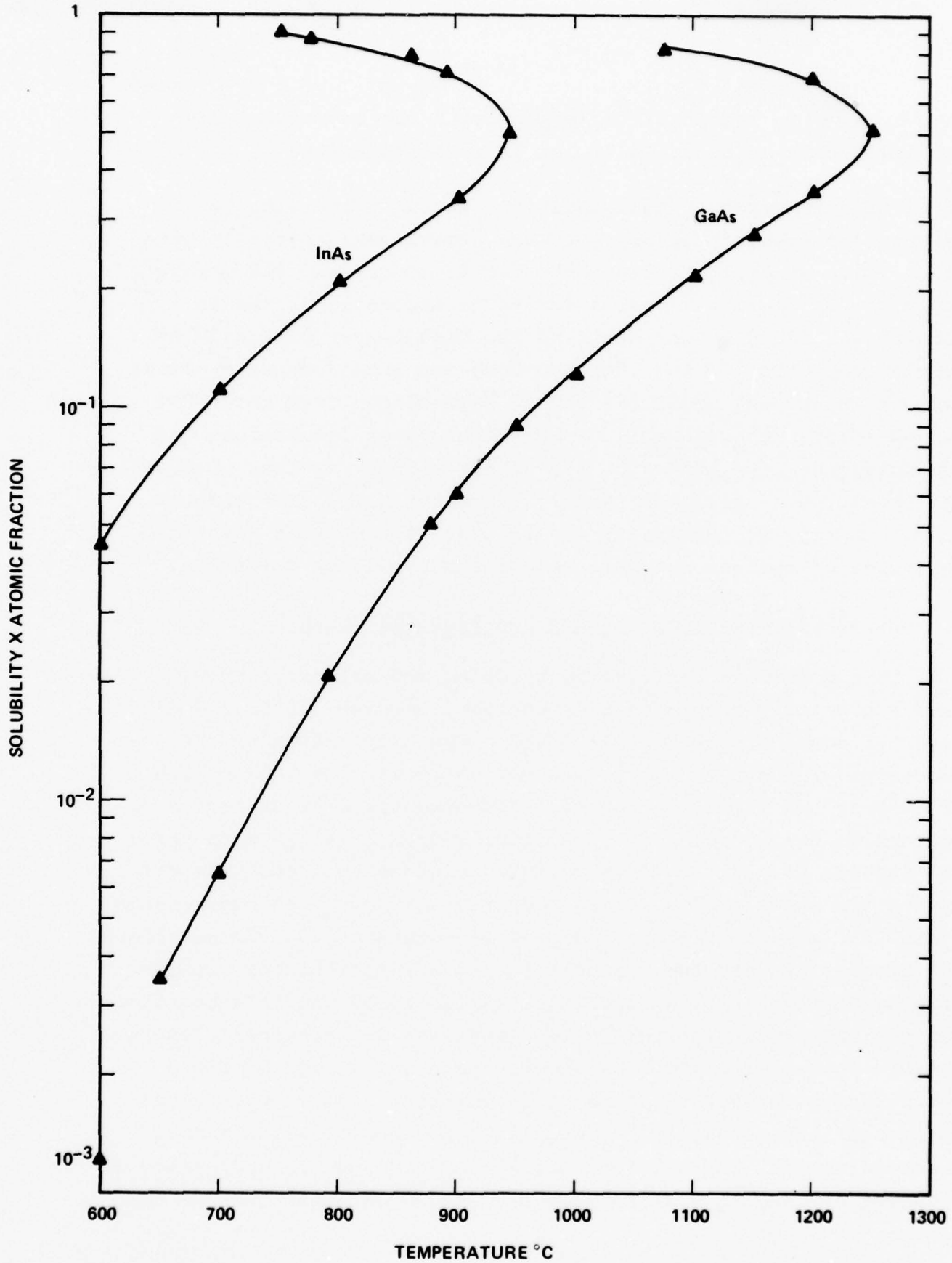


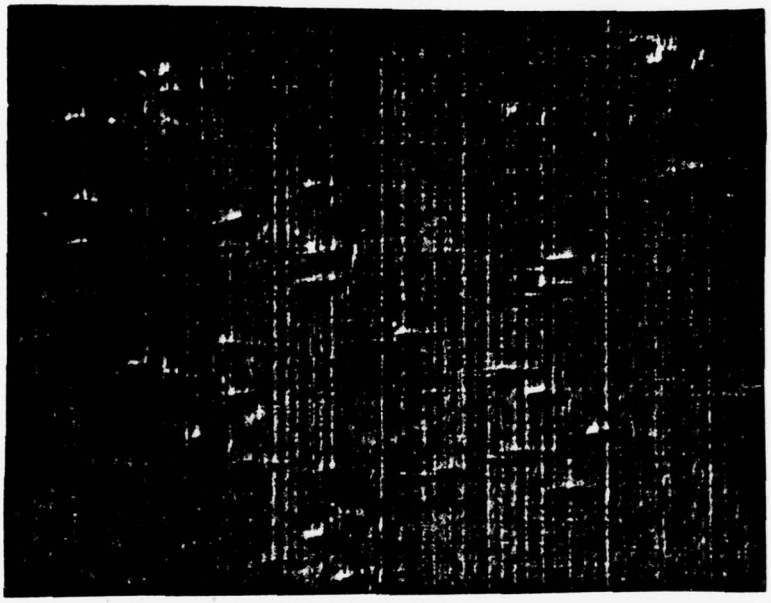
Fig. 4. Solubility curves for As dissolution in In and Ga (after Hall, Ref. 22).

about 11 hr in reasonable agreement with the experimentally observed time of about 10 hr for In saturation with As.

After temperature equilibration, during which some desaturation occurs, the sources were resaturated initially with 300 cc/min of $AsCl_2/H_2$ flow over the In source and 100 cc/min over the Ga source. After a series of depositions, the In source was found to deplete from the high temperature side of the source boat. This situation does not interfere with normal growth in any way until the source size is depleted about 80% or so after a considerable number of hours of saturations and depositions. The effect on the growth surface is then observed as formation of hillocks running along the (110) direction as shown in Fig. 5. Reduction of $AsCl_3/H_2$ flow at this point in the life of the source seems to eliminate hillock formation.

2.2.2 Compositional Grading and Epitaxial Growth

During grading for lattice matching and epitaxial growth the substrate was kept at a temperature between 713°C to 725°C and the sources were kept at 780°C. The composition of the deposited $In_xGa_{1-x}As$ layers was varied by varying the $AsCl_3/H_2$ flow over the In and Ga sources. Experiments were conducted to determine the composition of epitaxial $In_xGa_{1-x}As$ as a function of fractional $AsCl_3/H_2$ flow ratio over the Ga source. The results are shown in Fig. 6 and compared with previous experimental data[17,24] and calculated values of Ban-Ettenberg.[23] Compositional grading to the desired composition was accomplished by continuously controlling the input flow ratios to Ga and In (according to the data shown in Fig. 6) by means of a dual-channel electrostatic-curve-following programmer. Both the In and Ga flows were varied to keep the total flow constant. Since the composition of the deposited $In_xGa_{1-x}As$ is governed by equilibrium thermodynamics, letting the flow rate change during compositional grading by keeping flow through one source constant changes the



100 μm

Fig. 5. Hillock formation with high flow rates and small source volume.

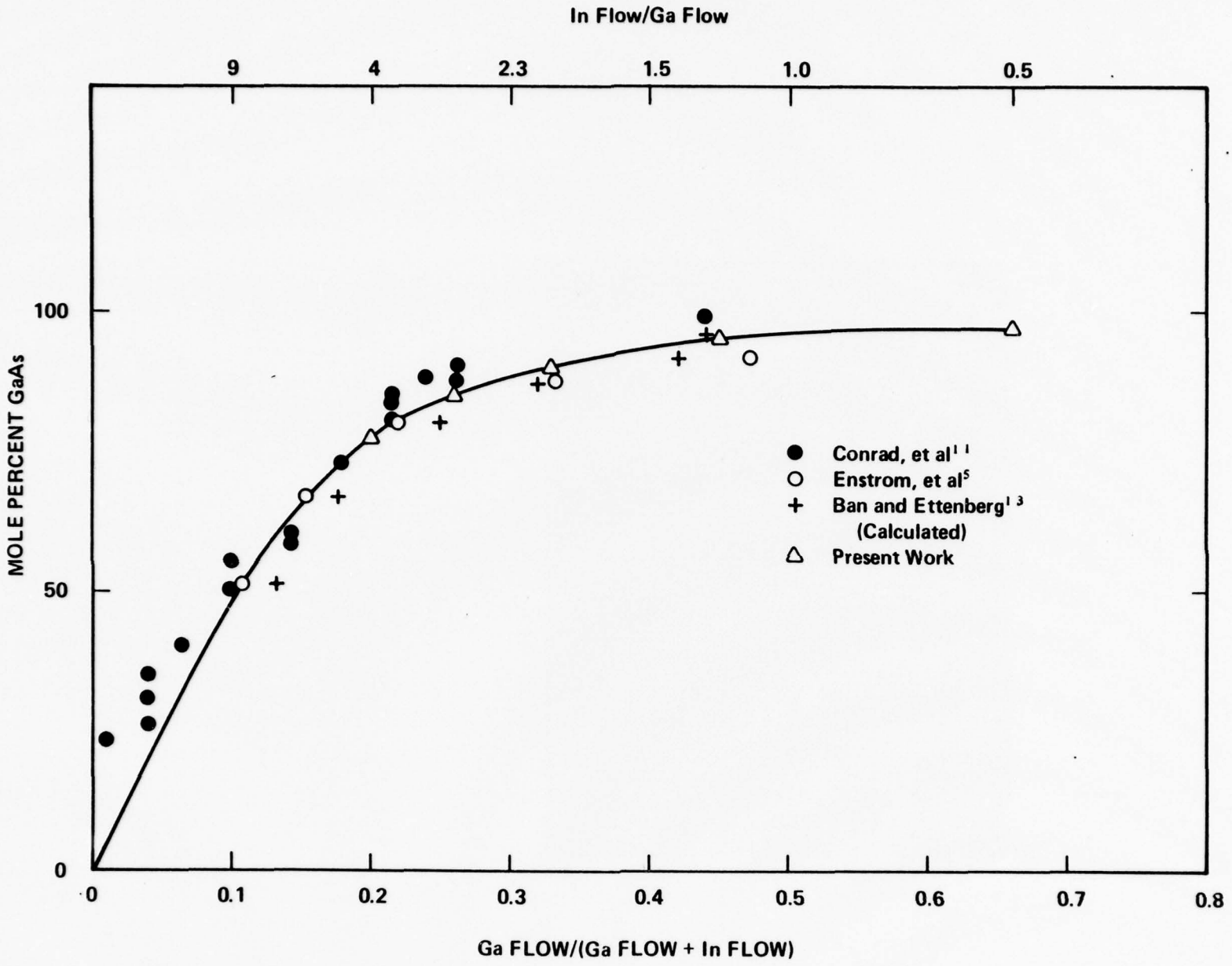
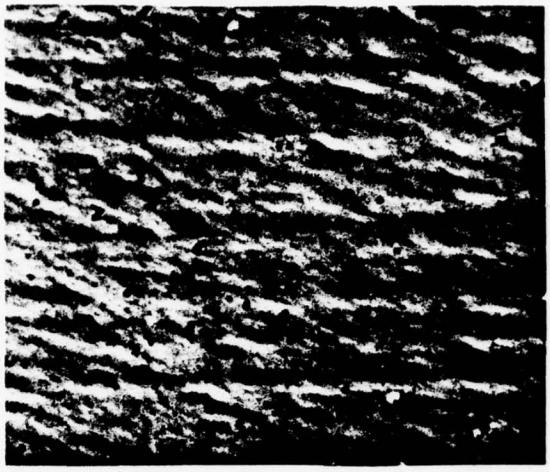


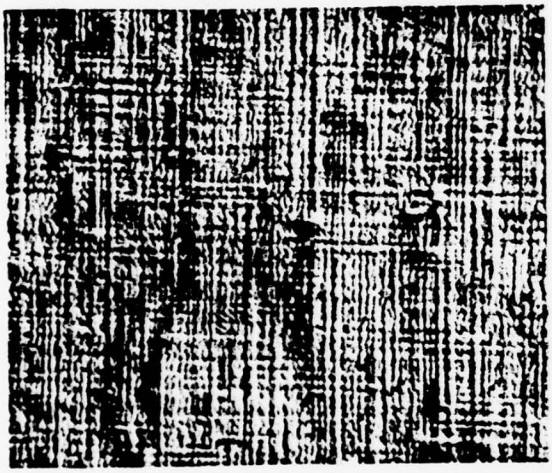
Fig. 6. Variation of epitaxial $In_xGa_{1-x}As$ composition with $AsCl_3/H_2$ flow over Ga and In.

growth rate during grading and results in degradation of surface quality and of electrical properties. Figure 7 shows the surface of epitaxially grown $In_xGa_{1-x}As$ with 14 mole% InAs, with (a) ungraded growth, (b) with 1 micron of graded layer, and (c) with 3.9 microns of graded layer. The better quality of the 3.9-micron layer grown with constant flow rate is immediately obvious. Figure 6 shows the electron mobility at 300°K of some of the films grown with different thickness of graded layers and ungraded growth. The material was doped to about $10^{17}/cm^{-1}$ electron density with H_2S. The graded layer was made semi-insulating with Cr doping using CrO_2Cl_2 as indicated in Fig. 3. The best results were obtained for graded layers of > 3-micron thickness using constant total flow rates, with mobilities of 6920 and 6840 $cm^2/V\text{-sec}$, indicated by 4-9 and 4-8 in Fig. 8. Samples 4-11 and 4-10 were also grown with constant flow rates, but the graded layers were only 2.5 microns and 2.8 microns thick, respectively. Specimen 4-1 has a 2.5-micron graded layer, but the flow rate was not constant throughout the grading. Effect of both variable flow rate and smaller graded thickness is depicted by Specimen 4-4 with a room temperature mobility of only 2770 $cm^2/V\text{-sec}$. The higher InAs concentration in this specimen with improper grading and gas flow rate also contributes to lower mobility. $In_xGa_{1-x}As$ grown directly on the GaAs substrate is exemplified by Specimen 3-15. The mobility is 4190 $cm^2/V\text{-sec}$ as compared with about 5200 $cm^2/V\text{-sec}$ obtained by Glicksman et al.[18] but is better than Specimen 4-4 and 4-1 only because the InAs mole% is much smaller, and lattice mismatch is not too large (0.3% as compared to about 1.4%).

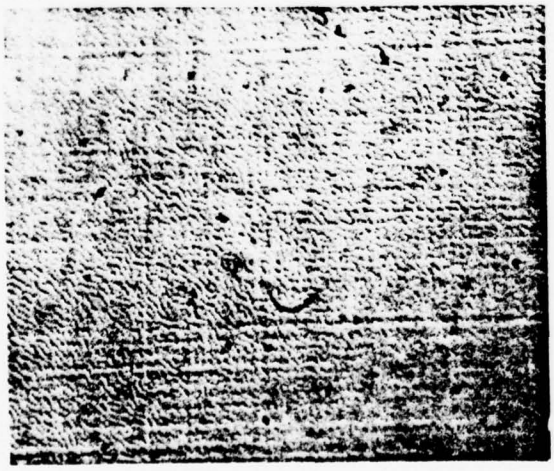
CrO_2Cl_2 flow of about 3.4×10^{-7} mole/min was used for doping graded layers which yielded epilayer resistivity of the order of 2×10^8 ohm-cm with a total $AsCl_3/H_2$ flow of 460 cc/min. When lower total $AsCl_3$ flows were used, surface



(a) Ungraded.



(b) 1 μm graded layer.



(c) 3.9 μm graded layer.

10 μm

Fig. 7. Surface of epitaxially-grown $In_{.14}Ga_{.86}As$ grown on ungraded and lattice-matched graded layers.

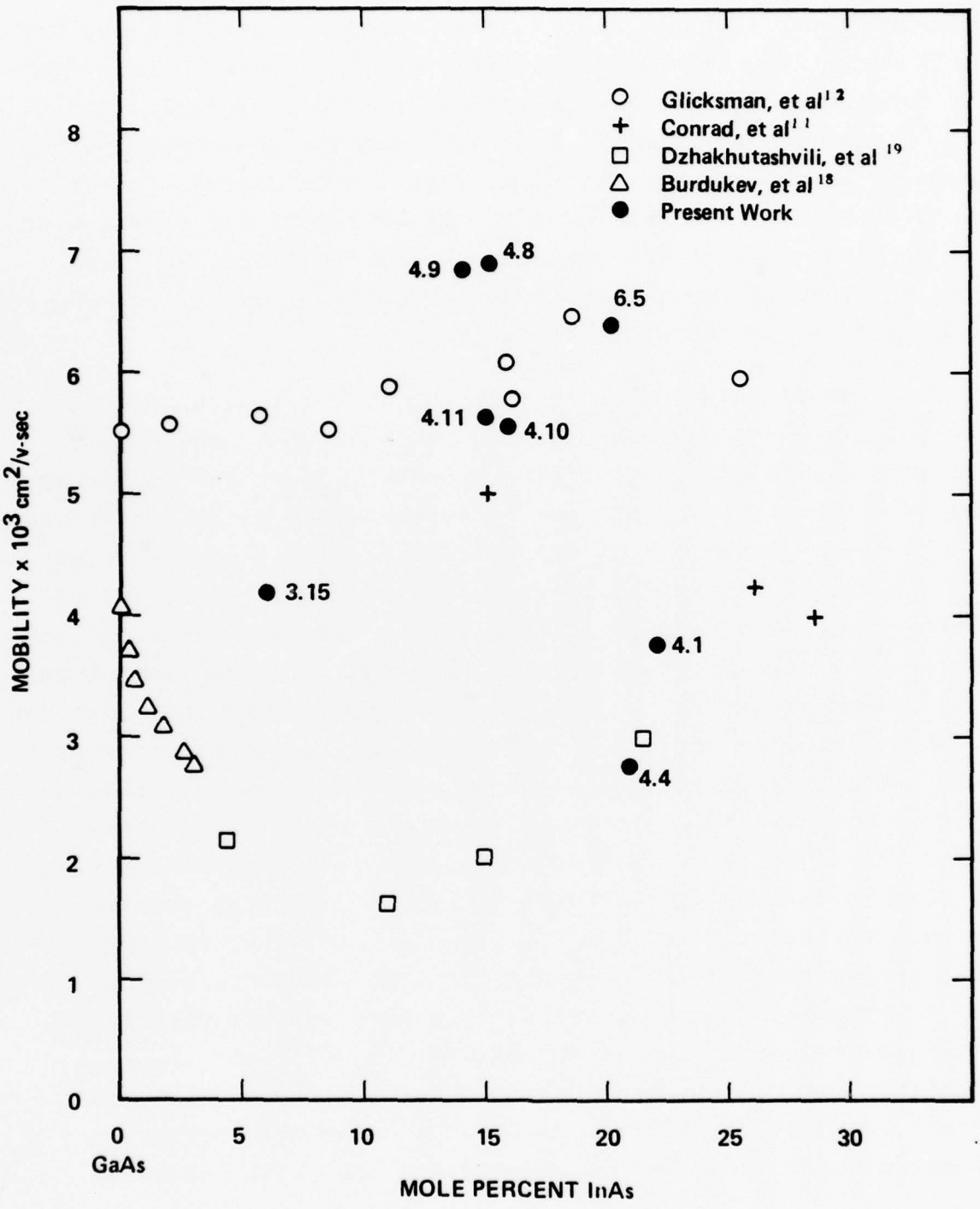


Fig. 8. Hall mobility as a function of mole percent InAs.

imperfections, shown in Fig. 9, were observed running along the (110) direction. These are possibly due to excessive Cr. Similar imperfections have been observed by Mizuno, Kikuchi, and Seki[25] and were attributed to Ga_2O_3 formation when water vapor produced in the reaction reacting with the Ga source. Since the CrO_2Cl_2 does not pass over the Ga source in our arrangement, the defects observed are tentatively attributed to the formation of stoichiometric CrAs which is found to give needle-shaped precipitates in Czochralski-grown GaAs.[26]

To establish desirable equilibrium growth conditions with the InGaAs system described in Fig. 3, the input $AsCl_3$ vapor pressure was adjusted by varying the $AsCl_3$ vaporizer temperature. Complete conversion of HCl to the monochloride of In and Ga was determined by placing a GaAs substrate partially covered with SiO_2 in the high temperature zone and measuring the amount of material etched. Increasing $AsCl_3$ vapor pressure was found to increase etching due to increased HCl production while at lower $AsCl_3$ vapor pressures, growth occurred at the substrate. Figure 10 shows the etch rate as a function of $AsCl_3$ vaporizer temperature. Complete conversion seems to occur at a vaporizer temperature of about 11°C, below which growth occurs in the high temperature region. Since in this series of experiments CrO_2Cl_2 is also used to provide Cr doping, extra HCl enters the reactor through the reaction of CrO_2Cl_2 and H_2. Use of an $AsCl_3$ vaporizer temperature of 11°C can therefore cause severe etching of the substrate. Figure 11 shows the growth surface with $AsCl_3$ vaporizer temperature of 11°C and CrO_2Cl_2 addition. An $AsCl_3$ vaporizer temperature of 7°C was therefore selected for the growth of material reported here, as a compromise between smooth etching, complete conversion and low growth rates.

Typically, S-doped $In_xGa_{1-x}As$ epitaxial layers with electron densities of the order of 10^{17} cm^{-3} were grown on semi-insulating GaAs (100) wafers oriented about 2° off axis

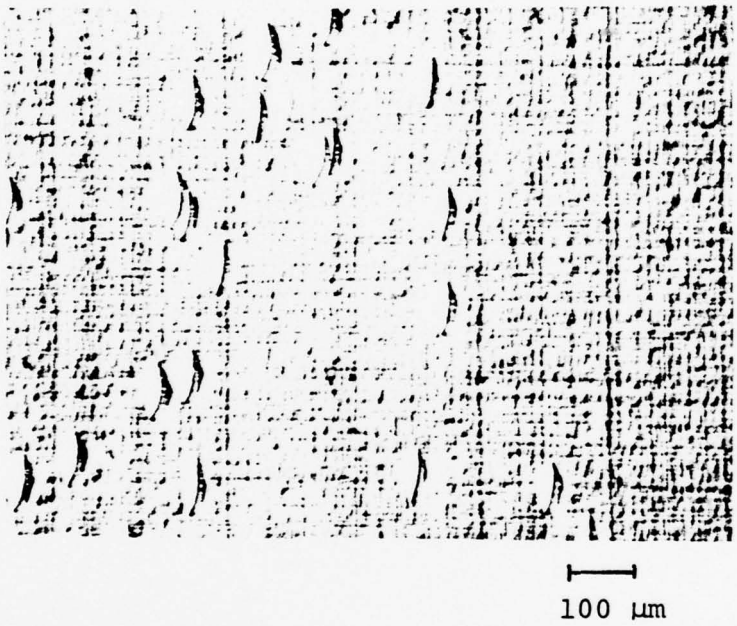


Fig. 9. Surface defects formed at high CrO_2Cl_2 flow.

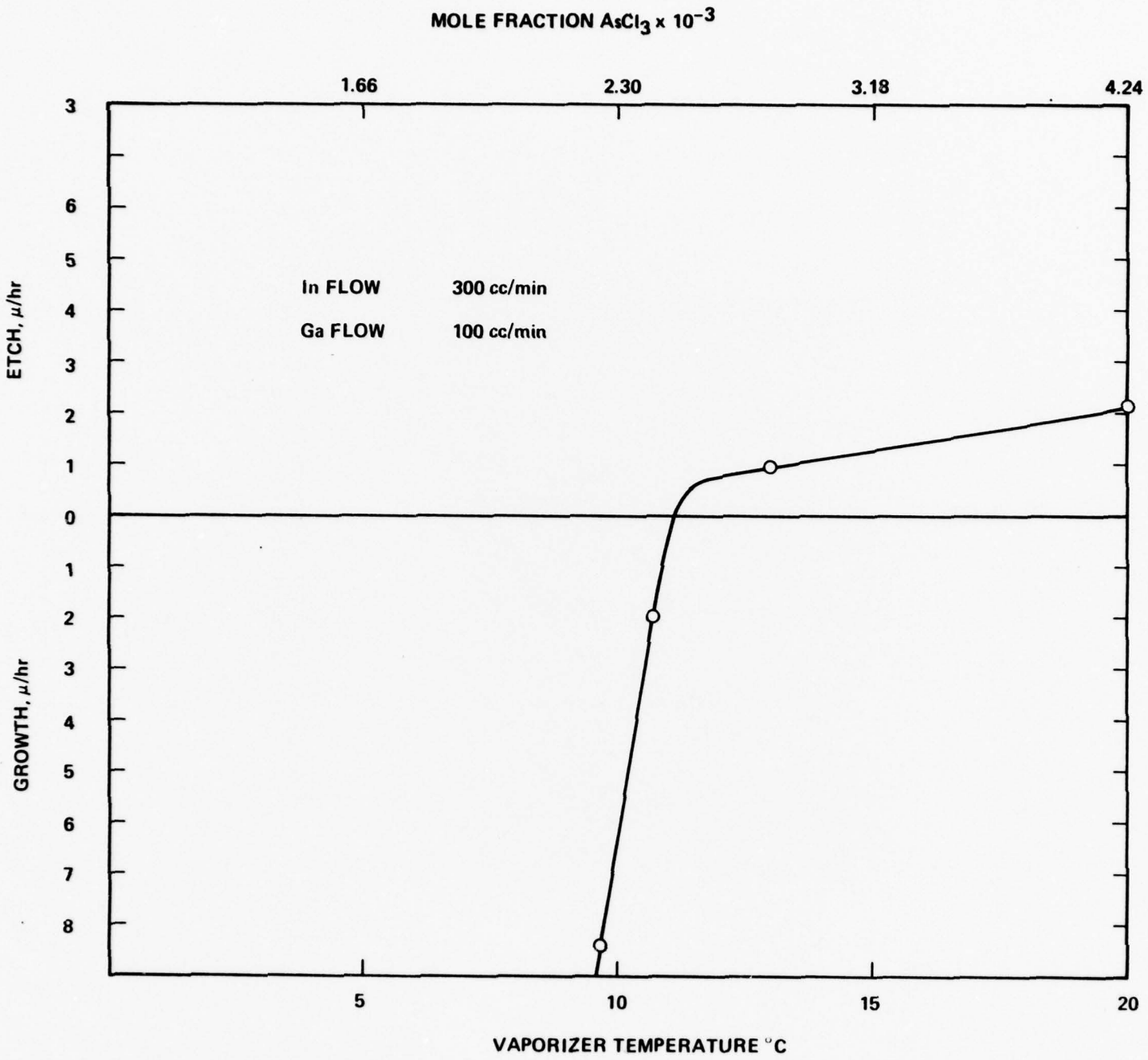


Fig. 10. Etch and growth rate at high temperature as a function of mole fraction $AsCl_3$.

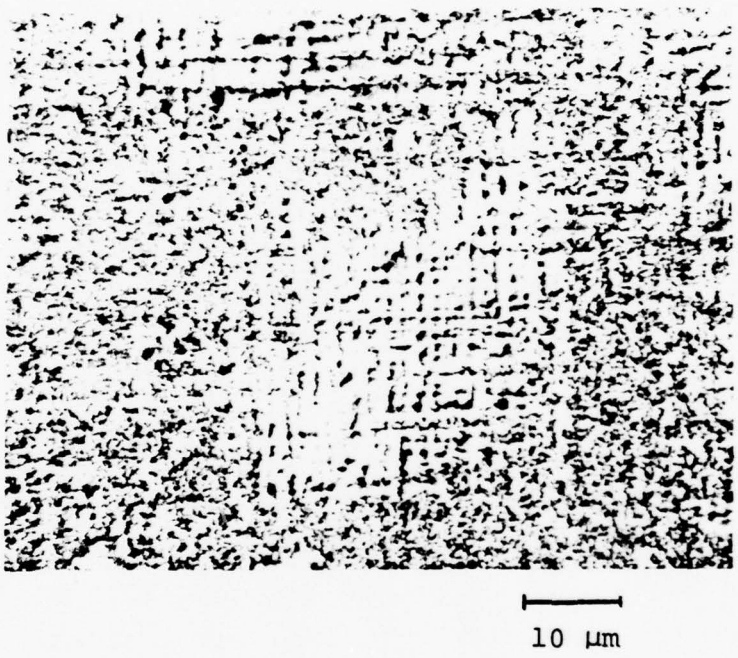


Fig. 11. Growth surface with the $AsCl_3$ bubbler at 11°C in the presence of CrO_2Cl_2.

towards the (110) plane. Graded layers for lattice matching were made semi-insulating with Cr doping. The GaAs substrate was placed in a horizontal position on the substrate holder and pushed into the hot zone during temperature equilibration and re-saturation of the sources. After HCl etch cleaning, the substrate was pulled back just beyond the S doping line (Fig. 3), and a graded layer grown on it to the desired InAs composition, as determined from the curve of Fig. 6. After a graded layer of about 3 microns or more was grown, the substrate was pulled further down in the deposition region where S-doped $In_xGa_{1-x}As$ was grown. This growth rate was found to depend on the total flow rate. For a typical flow rate of about 460 cc/min $AsCl_3/H_2$, the growth rate was found to be about 0.03 micron/min. A growth rate of 0.01 micron/min was obtained when the total flow rate was reduced to 260 cc/min. The growth rate during grading was typically 0.07 micron/min.

After the desired epitaxial growth thickness had been obtained, the doping line and $AsCl_3$ flow was shut off and the furnace rolled off from the reactor tube. The substrate was cleaned and stained to delineate the growth layers and the growth thickness was determined optically. Surface structure was observed optically under a Zeiss microscope. The electron density was determined using an impurity profile plotter. The InAs molar concentration was determined by measuring the bandgap[8] by photoluminescence and by x-ray diffraction determination of lattice constants. Hall mobilities were measured by the Van der Pauw method on square samples with alloyed In contacts on the corners. No correction for submicron layer thicknesses was made.

2.2.3 Materials Evaluation

Earlier measurements of electron mobility in melt-grown $In_xGa_{1-x}As$ with impurity concentrations of the order of $10^{17}cm^{-3}$ showed a drastic decrease in mobility with increasing concen-

tration of InAs.[27,28] This decrease in electron mobility was attributed to alloy scattering. A similar effect was observed by Ku[29] in $GaAs_{1-x}P_x$ with a carrier concentration of 1.5×10^{17} cm^{-3}. As opposed to $GaAs_{1-x}P_x$ (where a direct to indirect bandgap crossover occurs at $x = 0.44$[30]) $In_xGa_{1-x}As$ has direct bandgap through all compositions from GaAs to InAs. The expression for the variation of bandgap with InAs concentration is given by Nahory, Pollack, and DeWinter.[31] The energy of the Γ conduction band minimum in $In_xGa_{1-x}As$ decreases rapidly with increasing x whereas the energy of the X minimum increases slowly. The electrons are also characterized by decreasing effective mass as x increases. Experimentally determined conduction band effective masses have been found by Fetterman, Waldman, and Wolfe[32] to decrease linearly with increasing InAs concentration. The decrease in electron mobility observed in melt-grown alloys is too large to be explained on the basis of alloy scattering and is probably due to material being inhomogeneous. Purer and more homogeneous material grown from vapor has been shown to have a less marked decrease in mobility (Conrad, Hoyt, and Martin,[17] and Fetterman, Waldman, and Wolfe[32]). Glicksman et al.[18] on the other hand found practically no effect of composition up to a composition of $x = 0.25$ InAs. In Fig. 8 the data points labelled with sample numbers show the mobilities obtained in some good and bad samples of thin film $In_xGa_{1-x}As$, all grown from vapor with a donor concentration of the order of $10^{17}cm^{-3}$. Results of other work reported in the literature are also shown for comparison. All the alloy layers grown in the present study were of the order of a micron or less in thickness as shown in Table II, and the graded layers for compositional lattice matching were made semi-insulating as indicated earlier.

Our data do not confirm the downward trend in mobility with increase of InAs content noted in earlier literature. In this respect, our results agree with those of Glicksman

TABLE II

Sample #	Thickness: Grading (μm)	Thickness: Epitaxial (μm)	InAs Conc. x (%)	Resistivity (Ω-cm)	Hall Mobility 300°C (cm^2/Vsec)	N_D-N_A (Hall) (cm^{-3})	Carrier Conc. (Differential Capacitance) (cm^{-3})
4-1	3.5	0.7	23	.002	3750	7.62×10^{17}	7.8×10^{17}
4-4	1	0.3	22	.028	2770	3.51×10^{16}	1.5×10^{17}
4-8	3.4	0.53	15	.015	6920	5.9×10^{16}	1.1×10^{17}
4-9	3.9	1.0	14	.016	6840	5.62×10^{16}	1.2×10^{17}
4-10	2.8	0.4	16	.01	5560	1.15×10^{17}	1.8×10^{17}
4-11	2.5	0.35	15	.037	5630	3×10^{16}	1×10^{17}
6-5	2.9	0.7	20	.015	6360	6.4×10^{16}	1.2×10^{17}
3-15	---	0.5	6	.33	4190	4.46×10^{15}	1.5×10^{17}

et al.[18] On the other hand, quality of the surface and quality and thickness of graded layers seem to affect the electrical properties. For slow growth rates that were used, a thickness of the graded layer of about 3-5 microns seems to be sufficient. Using constant flow rates, as mentioned in an earlier section, also seems to improve the quality of the film. Sample 3-15 was ungraded and seems to have a moderately highly compensating acceptor impurity. Sample 4-1 was grown on an undoped graded layer. It is seen from these results that for a properly grown $In_xGa_{1-x}As$ layer such as, for example 4-8 and 4-9, the room temperature mobility is higher than previously reported for any alloy of comparable composition and carrier density. The degradation in mobility seems to be only due to inhomogeneity and other structural disorders in the epitaxially grown alloys.

Efforts to increase the InAs concentration to 50% were not entirely satisfactory owing to excessive depletion of the In source. However, a layer with 35% In was grown with a doping level of 10^{17} cm^{-3}.

2.2.4 Source Size, Source Saturation, and Graded Layer Studies

InGaAs was grown by the two-source method with 500 cc/min total flow of $AsCl_3N_2$ for the study of the source size effect. The sources, which weighed 50 g each, had a surface area of about 12 cm^2. Since a shunted single-zone furnace was used, a temperature gradient existed over the sources. Near the up-stream portion of the source the gradient was about 0.2°C/cm and progressively increased to about 1°C/cm near the downstream side, which was at a higher temperature. Compositional grading was accomplished by controlling the respective H_2 flows through the Ga-$AsCl_3$ and In-$AsCl_3$ bubblers which were held at 7°C. The graded layers were Cr-doped and the active layers were doped n-type using 310 ppm H_2S in H_2 as a dopant, to give a final

net carrier concentration of $\sim 10^{17}$ cm^{-3}. The material was evaluated for surface quality and composition by optical microscopy, x-ray topography, and x-ray diffraction for lattice constant measurements. The electrical properties were determined by the Van der Pauw method and by a C-V impurity profile plotter.

It has been pointed out by Clarke[33] that a source skin dissolution mechanism is important in growth of InP with low background doping. A similar effect evidently occurs in the Ga source as well as in the In source but because the Ga source is usually of higher initial purity, the effect of Ga skin dissolution on the doping level is not drastic. With the two-source system of InGaAs growth, skin dissolution in the In source effects the background doping if a temperature gradient exists over the sources. This temperature gradient also causes the depletion of the source from the high temperature side, thus reducing the surface area exposed to reaction with the $AsCl_3$/HCl flow. Surface quality and growth are also affected by InAs crust dissolution.

For a furnace temperature profile that has gradients at the source position, the decreasing size of the In source decreases the growth rate and also affects the composition of the material grown, mainly because of incomplete reaction with a smaller source. This effect of decreasing size of the In source on the percentage InAs in InGaAs for three constant flow ratios Ga flow/Ga+In flow of 0.1, 0.16, and 0.2 is shown in Fig. 12.

The effect of compositional grading and the thickness of the graded layer on the surface quality of vapor-grown InGaAs has been discussed previously. It was observed that with graded layer thicknesses from 2 to 4 microns, active layers with good quality surfaces can be grown for FET fabrication. Larger graded layer thickness shows a slight improvement in

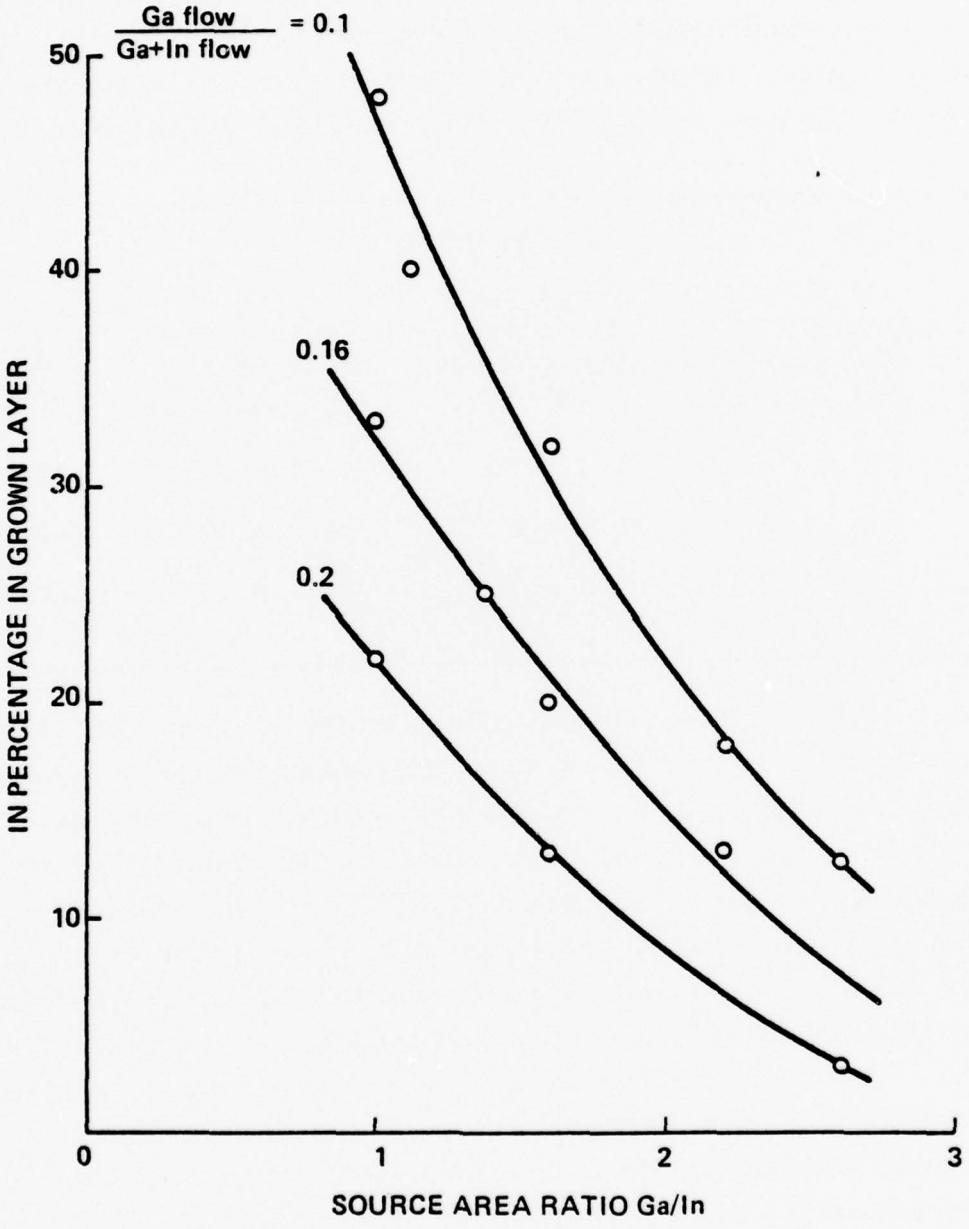


Figure 12. Indium percentage in grown layer as a function of source size for a constant total flow ratio Ga/(Ga+In).

surface quality; however the structural quality seems to improve appreciably with thickness, as observed in x-ray topographs.

The electrical properties of the active layers also appear to improve considerably when the material is grown on thicker graded layers. Table III shows the electrical characteristics of three typical wafers with 2.8, 3.9, and 7.1 micron thick

TABLE III

InGaAs Wafer #	Conc. InAs (%)	Grading (μm)	Carrier Conc. Diff. Capacitance (cm^{-3})	N_D-N_A Hall Data (cm^{-3} 77°K)	Mobility (cm^2/Vsec) 300°K	Mobility (cm^2/Vsec) 77°K
4-10	16	2.8	1.8×10^{17}	1.09×10^{17}	5560	7080
4-9	14	3.9	1.1×10^{17}	4.6×10^{16}	6840	11200
11-9	20	7.1	3×10^{16}	2.08×10^{16}	8980	22760

graded layers. The n-doped InGaAs material with 20% InAs concentration grown on a high resistivity compositionally graded layer of 7.1 micron thickness showed the highest mobility yet reported for vapor-grown material, with room temperature mobility of 8980 cm^2/V-sec and a mobility of 22760 cm^2/V-sec at 77°K. A higher mobility than this has only been reported in $In_{.53}Ga_{.47}As$ grown by LPE.[15] Figure 13 gives the C-V impurity profile of this wafer and shows the thickness and doping level of the active layer. The two other specimens in Table III show decreased mobility and increased compensation in the active layer with lower thickness of the Cr-doped graded layer. This indicates that compensation in material grown on thinner graded layers is probably due to dislocations in the material produced by too fast a grading rate. A grading rate of 2.8% InAs/micron (as in specimen #11-9) with a growth rate of about 2 microns/hr appears to yield good quality material in the present system.

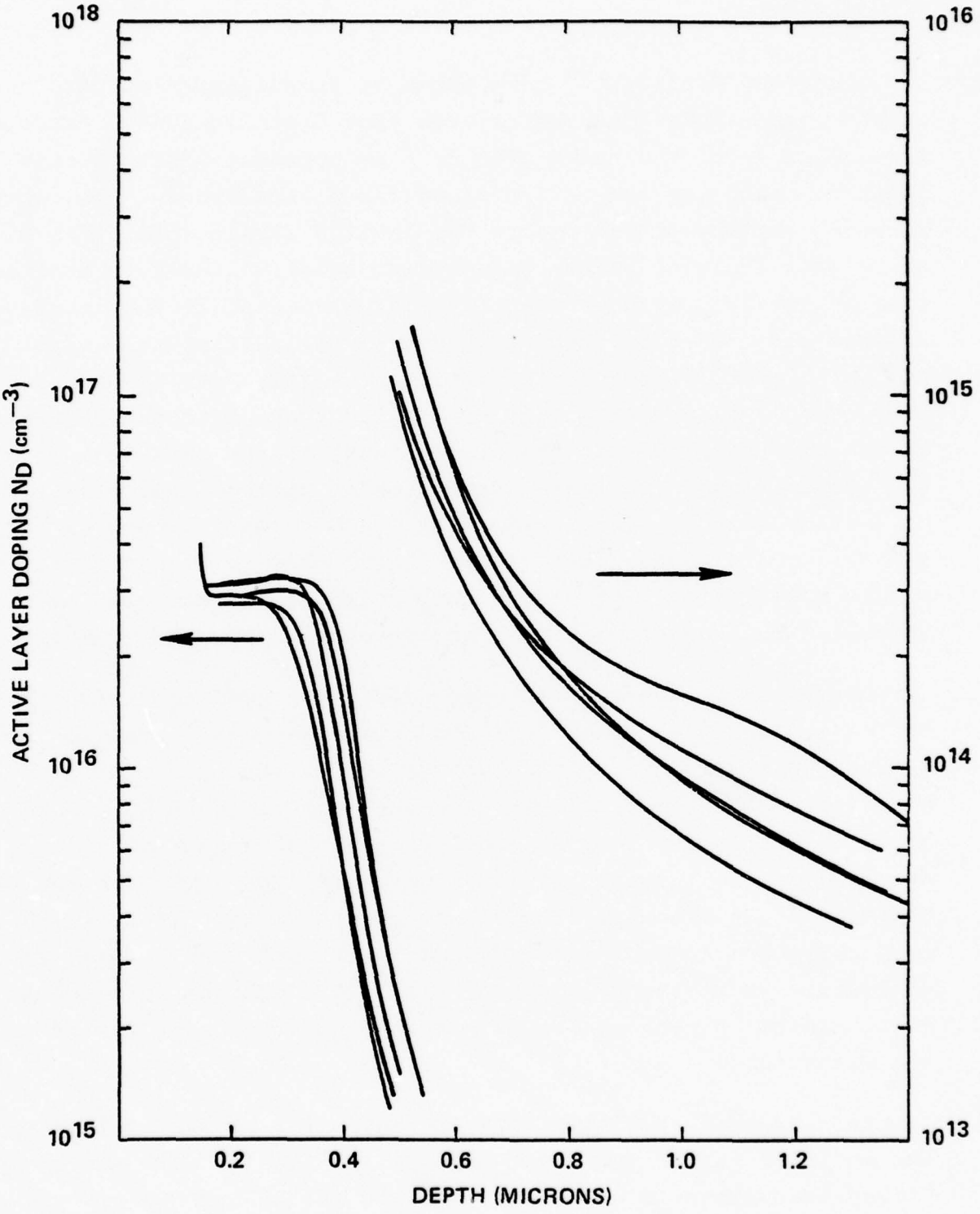


Figure 13. Doping profile of high mobility $In_{.2}Ga_{.8}As$ wafer.

Olsen and Ettenberg[34] have shown by transmission electron microscopy of InGaP-GaAs interfaces that a strain due to lattice-mismatch $\Delta a/a$ of the order of $\leq 10^{-4}$ is apparently required in order to avoid any generation of misfit dislocations. Slow compositional grading should reduce the lattice strain considerably below this limiting value, but Enstrom et al.[24] indicate that in case of InGaAs growth on GaAs, a grading rate of 1% InAs concentration per 1 micron of growth is still not sufficiently small enough to avoid mismatch dislocations entirely. Abrahams and co-workers[35] show that misfit dislocations are introduced during grading and their density is proportional to the magnitude of the compositional gradient. These misfit dislocations give rise to inclined dislocations which were found to bend in and out of a misfit plane. When bent in, they give rise to stress-relieving misfit dislocations, otherwise they propagate effectively even through a constant composition region grown after the grading.

Our observations show a lower density of grading dislocations on the surface than at or near the interface when a grading rate of 2.8% InAs micron^{-1} is used with a growth rate of about 2 microns/hr. Although the lower dislocation density is due to bunching of dislocations already created, the higher mobility attained in the specimen (#11-9) indicates improvement in the quality of the material with slower growth rates. It is therefore possible that both lower grading rate and lower growth rates contribute to better quality material and a compromise between these has to be made to attain a practical time of growth of the material.

In view of this study, the VPE system for growth of InGaAs was modified in various ways. A two-zone furnace with sodium-filled heat pipes is now used to obtain a flat-temperature profile at the sources and to thus overcome the reoccurring problem of a high background doping in the graded buffer layer.

2.3 Two-Source System with Heat Pipes

Changing to a sodium-filled heat pipe type of furnace involved a considerable delay due to repeated exchanges of faulty equipment. After the furnace was finally installed and operating properly, it was necessary to conduct experiments to re-establish the proper conditions for FET growths.

As can be seen in Fig. 14, the new reactor profile is very flat in the source area with a total source temperature variation of 0.1°C. This effectively eliminated the crust dissolution problem in the InAs source which was discussed above. As a consequence, the doping caused by impurities in the exposed In metal was eliminated, allowing semi-insulating Cr-doped layers to be produced repeatably and reliably.

In the course of seeking the proper reactor operating conditions, layers with grading rates from 0.9% to 4.9% InAs/micron were grown. Growth rates ranged from 0.2 to 9 microns/hr. The layers were analyzed by optical microscopy and photoluminescence spectra.

Device quality surfaces were obtained at grading rates of 3%/micron and below. A layer graded with a 4.9% InAs/micron rate to 15% InAs showed marked cross-hatch effects on the surface due to lattice mismatch strain. Satisfactory results were obtained with a grading rate of ~ 3 microns/hr and a growth rate of 2-4 microns/hr. The buffer layer growth rate was optimized by locating the maximum growth point in the reactor and then adjusting the furnace and sources with respect to the tube in order to position this point correctly for the buffer layer growth. The growth was also improved by etching off all wall deposits prior to each run. It was necessary to ensure that the growth rate did not exceed about 5 microns/hr, otherwise terraced deformities began to form in the layer and its structural quality deteriorated.

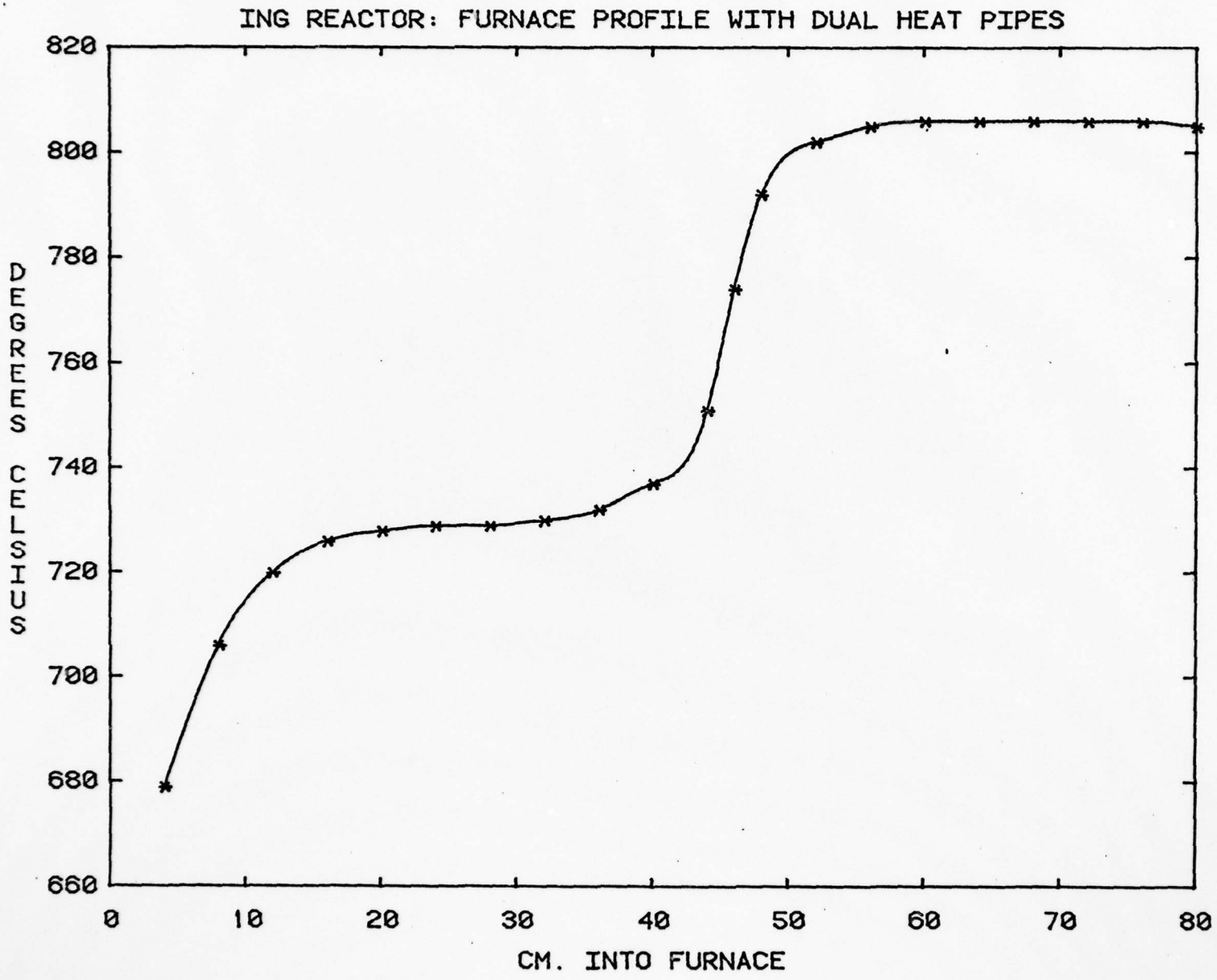


Fig. 14. Reactor furnace temperature profile with dual heat pipes.

Figure 15 shows a study of the % InAs vs Ga/(Ga+In) flows from this work. The results shown are consistent with and extend previous data in this area. The Ga/(Ga+In) flow for $In_{.25}Ga_{.75}As$ is seen to be Ga/(Ga+In) $\simeq$ 0.18.

Inspection of Table IV shows evidence of the effect of In source depletion on the epi layer composition. For InG #17-4, InG #17-6, and InG #17-7, the Ga/(Ga+In) flow remains nearly the same yet the % InAs in the resultant layer is drastically reduced. For InG #17-6, the % InAs is 4.6 with a Ga/In+Ga flow of 0.20. To achieve this same % InAs with a Ga/In source size ratio of 1 would require a Ga/Ga+In flow of ~ 0.50. From this it can be shown that approximately 75% of the HCl passing the In source did not react in InG #17-6.

TABLE IV

Run #	Approx. Source Size Ratio (In/Ga)	Ga/(Ga+In) Flow	%InAs	PPM H_2S	N_D-N_A/cc
17-4	0.8	0.21	18	0.18	$< 10^{16}$
17-6	0.6	0.20	4.6	0.81	$4x10^{16}$
17-7	0.4	0.18	3.9	1.52	$\sim 5x10^{16}$
17-8	0.3	0.12	0	1.52	---

When the Ga/In source size ratio decreases, i.e. when the InAs source begins to deplete, there is evidence of a considerable effect on the doping. Apparently the excess HCl present in the growth region due to incomplete reaction at the InAs source causes a reduction in the doping level. This is consistent with the results of Nozaki et al.[69] Table IV shows this effect on a series of runs made with a depleted source.

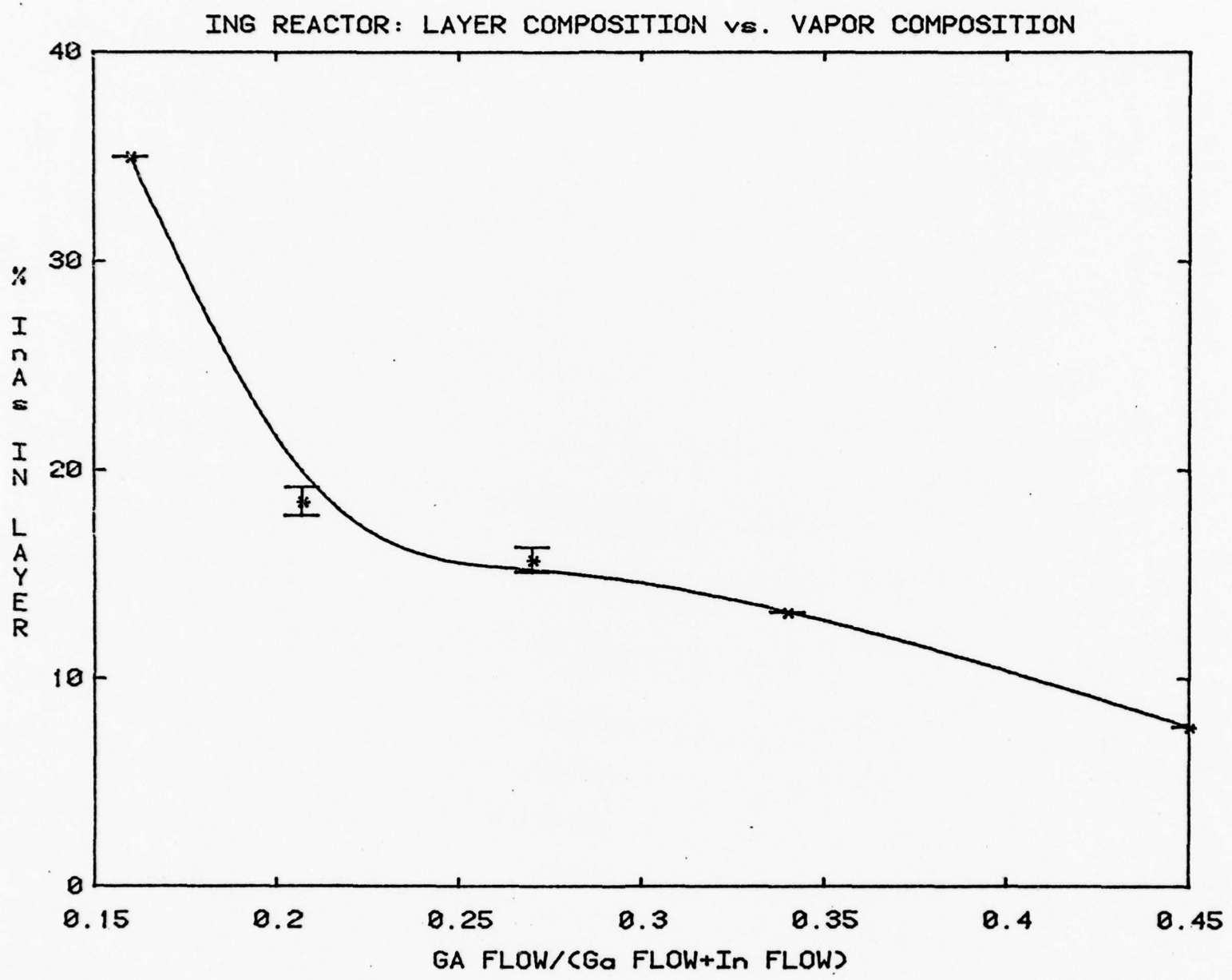


Fig. 15. Layer composition vs vapor composition.

2.3.1 Doping Problems with the Buffer to Active Layer Transition

The first full FET runs in the new system produced no S-doped active layer. The reason for this was discovered to be that the doping system was not responding correctly and the H_2S dopant was not being included in the growths for a period of 25 min after the doping system was turned on. Since this delay was longer than the entire active layer growth, no doping took place. This delay had existed previously but its effects had been masked somewhat by the high background doping due to the incomplete InAs crust resulting from the temperature gradient over the source. Indeed, it had been thought to have been eliminated by modifying the doping gas mixing manifold.

To counteract this effect, several runs were made with the H_2S doping system turned on during buffer layer growth. The buffer layer was grown upstream from the H_2S port to avoid doping. For active layer growth, the substrate was pulled back to a position downstream from the H_2S port. #InG 18-4 was one of the best of these runs, and Fig. 16 shows a doping vs depth profile obtained by C-V analysis of this run. The doping level and active layer thickness can be seen to be within the general tolerance for FET devices. However the doping at the buffer layer interface drops steeply only to 1×10^{17} and then begins to "tail" at a rate of 0.1 micron/decade or more. This is not suitable for fabrication of high performance FETs.

There were two primary reasons for the tail in the doping profile at the buffer layer interface. First, back-diffusion of S into the buffer layer growth area is possible when the H_2S line is on during buffer growth. This could alter the background level in the buffer layer as a function of the H_2S pressure downstream. Second, if the doping system was only beginning to respond when the active layer was grown, its slow rise time would

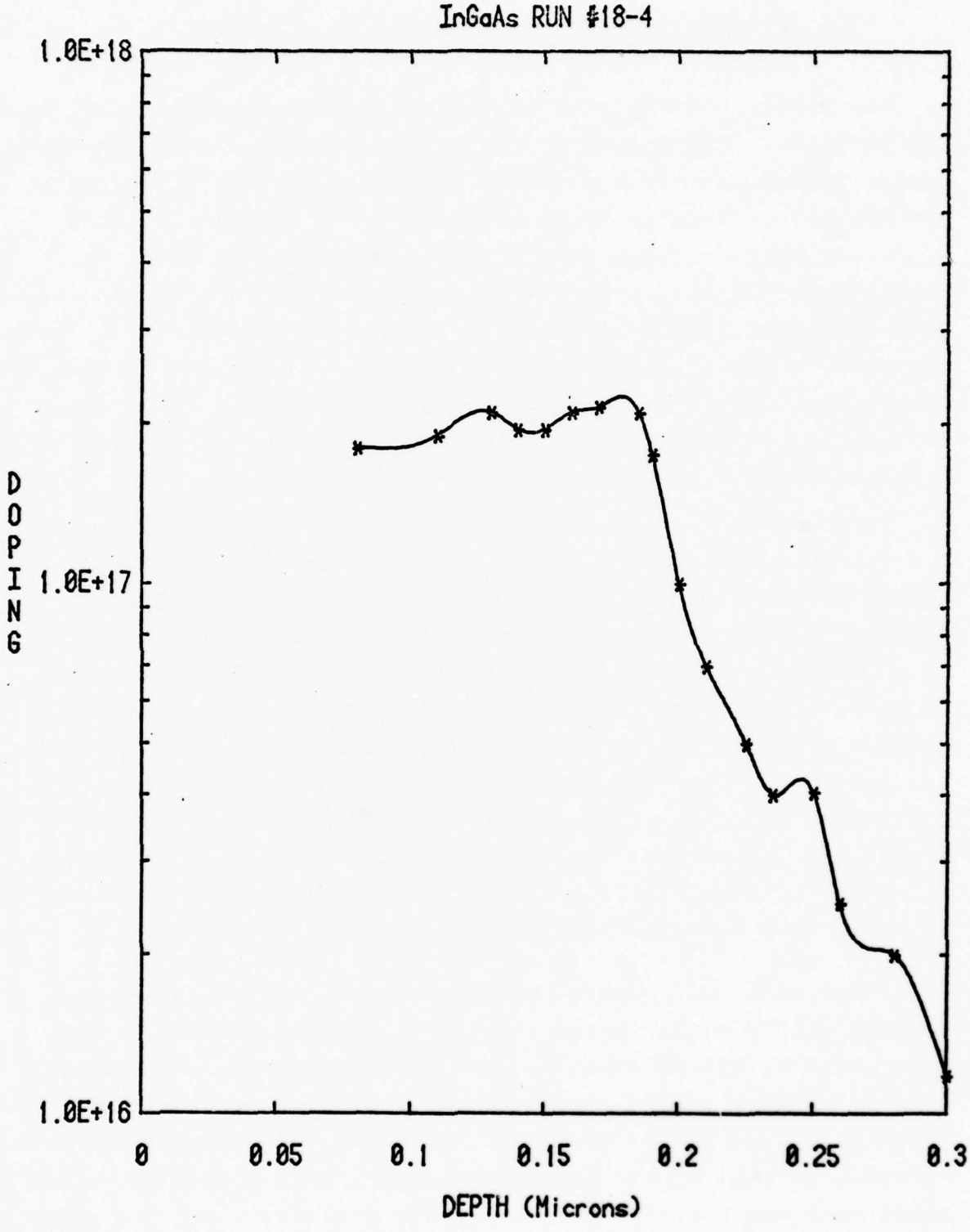


Fig. 16. Doping profile for wafer #InG18-4.

produce a slow rise in the active layer doping. Introducing a period of no-growth, no-etch into the run to allow the doping system to fully respond proved infeasible because the length of time involved necessitated far more precise control over the growth/etch condition than was possible at that stage of the run. It was necessary therefore to improve the doping system response of the system. Tests were performed that indicated that the doping delay was produced by irregularities in the doping system itself and was not a result of the thermodynamic reactions in the reactor, or Cr autodoping. As a result, the doping system was again modified by using smaller diameter tubing to reduce total system volume and tested for improved response.

In the meantime, until these modifications could be fully implemented, a two-run growth technique was tried. In this scheme the graded buffer layer was grown in one run and the active layer in another. By doing this the effect of the doping delay could be eliminated since there was unlimited time before active layer growth. Also, any possible autodoping by Cr-doped wall deposits could be avoided. The results of this technique were unsatisfactory however owing to the inability to avoid some lattice-mismatch between the buffer and the active layers. This produced a very poor interface and consequently the material was judged unsuitable for FETs.

When the delay in the doping system response persisted, it was necessary to make more radical improvements to the doping and the vapor etch systems. In the doping system the doping-gas/dilution-gas mixing chamber, which had simply been a four-way intersection of the input and output streams, was completely replaced by one designed to force greater mixing and avoid transient effects. This was accomplished by moving the two inputs away from the outputs and allowing a greater volume for mixing, as shown in Fig. 17. The result was an improvement in the doping system response time from 25 min to less than 4 min.

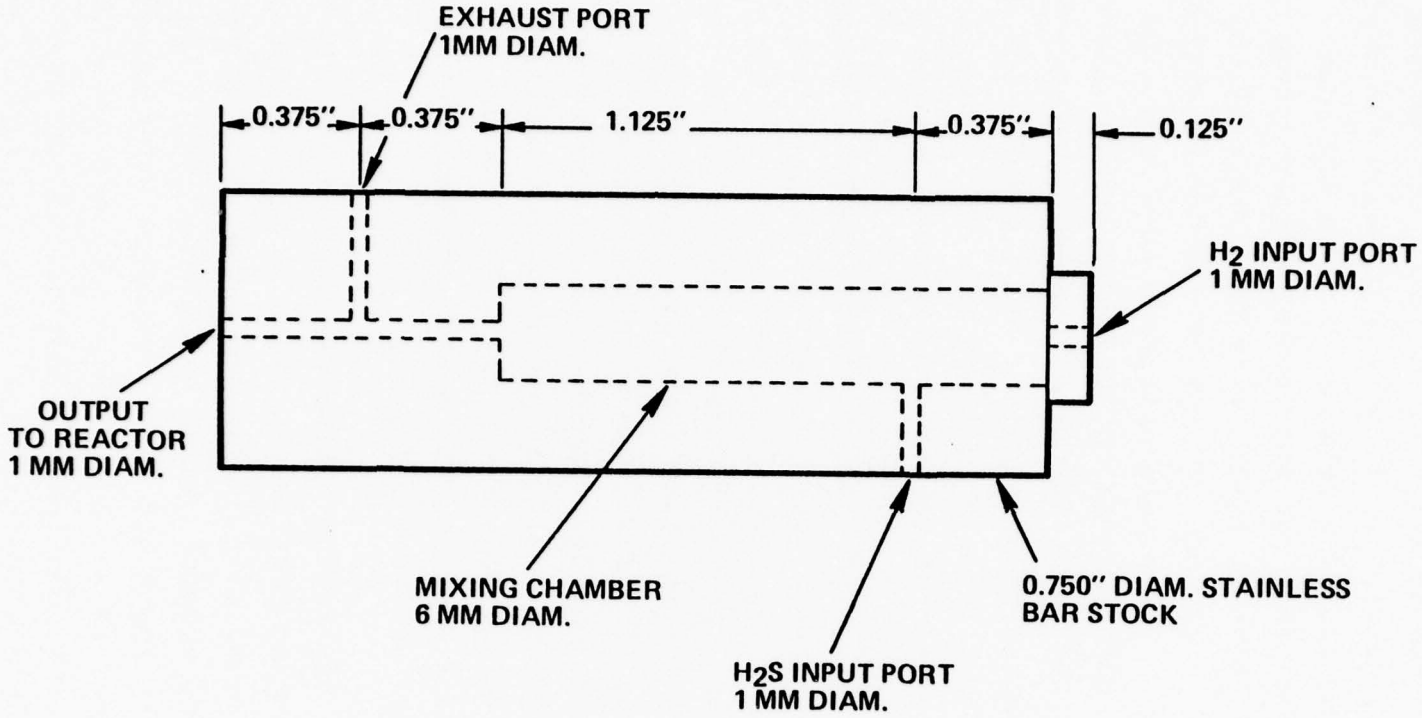


Figure 17. H_2S doping mixing chamber.

The new system showed very good repeatibility with respect to both response time and doping level, and it produced FET active layers with a flat doping profile for N_D-N_A on the order of 10^{17} cm^{-3} uniformly over the entire wafer. The modification to the vapor etch system was designed to boost the flow of HCl into the reactor during the doping level equilibration time. It was discovered that some growth was occurring during this time, which was causing the interface between the active layer and the semi-insulating buffer layer to be too wide. It is crucial to device performance that this interface be as thin as possible. The new system provides a light vapor etch during the doping system response time by boosting the HCl/(GaCl+InCl) concentration ratio to ~ 3/2. A comparison of the results of this system with the previous results can be seen by comparing Fig. 18 with Fig. 16. The new system produces a decade drop in doping in the space of ~ 600 Å which is comparable to that obtained for GaAs.

2.3.2 Growth Procedure Refinements

It was observed that the active layer thickness was nearly independent of growth time. From this it was deduced that the vapor in the reactor was severely depleted in the active layer growth position and growth was occurring only transiently after the wafer was moved from the buffer layer growth position. This problem was solved by moving the active layer growth position upstream 4 cm. To reduce the possibility of mismatch between the active layer and buffer layer due to transient effects, the wafer was moved to this position during buffer layer growth, 9 min prior to the start of active layer growth. Since these changes affected the active layer growth rate, and since active layer thickness must be very accurately controlled, recalibration of this rate was necessary.

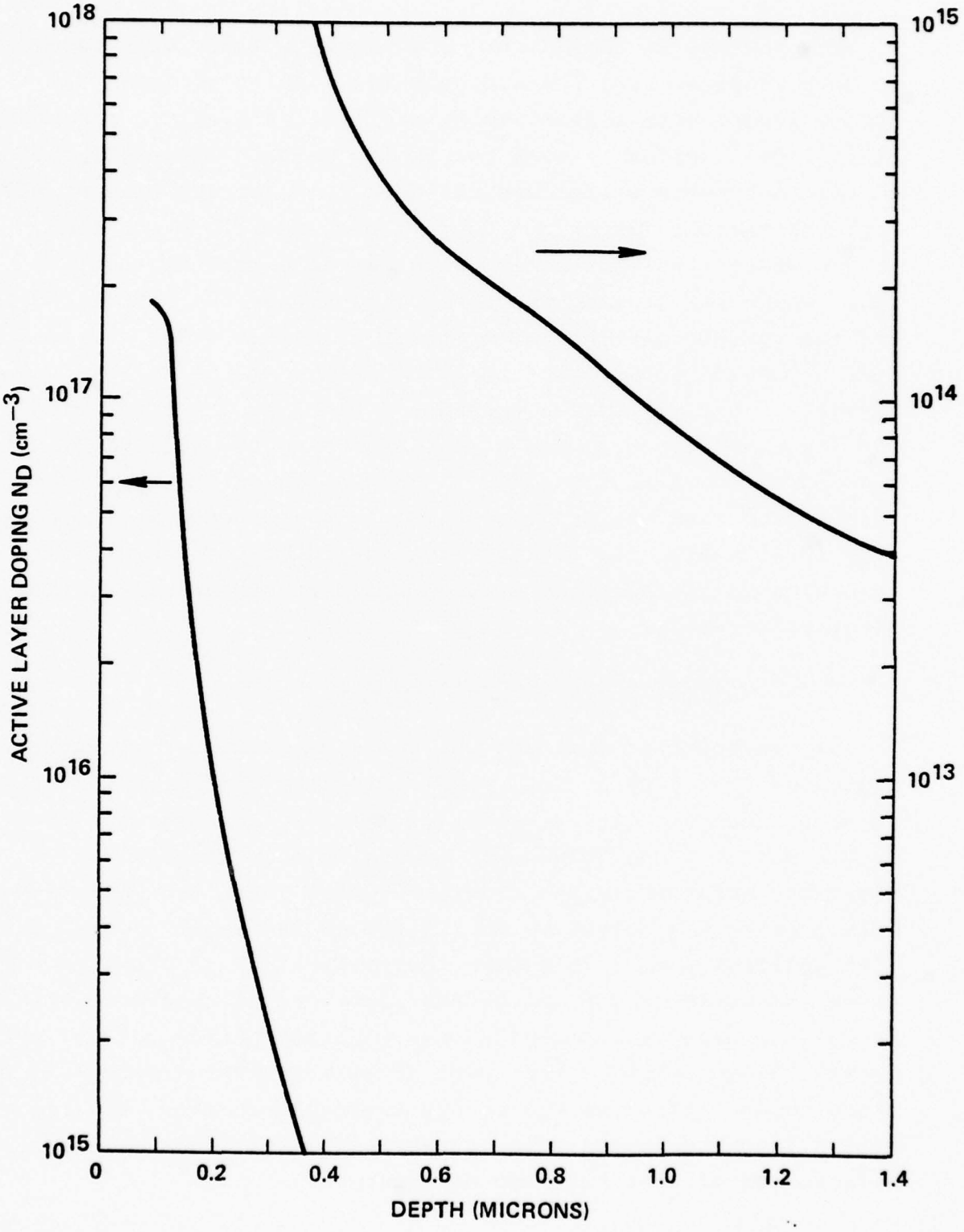


Figure 18. Doping profile for wafer #InG 20-11.

The active layer growth rate depends on several conditions in the reactor and especially on the substrate position and the amount of wall deposits in the reactor. Any change made in the buffer layer growth such as growth rate, percent In, thickness, etc. causes a different amount of wall deposit to be present during the active layer growth, thereby affecting the active layer growth rate. As the conditions for the buffer layer growth became more standardized and the correct position became known, the active layer thickness became more controllable, allowing the establishment of active layer growth rates of 0.05 micron/min for 15% InAs material and 0.035 micron/min for 18 to 19% InAs material. Once the active layer growth rate was calibrated, FET quality layers containing up to 19% InAs were grown. By using a slow grading rate of 2%/micron in conjunction with a slow growth rate, as explained above, it has proved possible to produce layers of better crystallographic quality than previously, even at the higher InAs percentages. Figure 19 shows the surface of a 15% InAs layer magnified 110x, with phase contrast adjusted to maximize deformities. This layer, which is one of the most recently grown, has one of the best surfaces yet produced. Step grading of the buffer layer was also tried in hopes of producing still better material. To date however layers produced by this technique have shown no visual improvement over those grown with slow continuous grading.

The doping profile of the InGaAs material has also been improved by experimenting to find the optimum doping response time and vapor etch conditions. The profile shown in Fig. 20 is very uniform at $N_D-N_A = 1 \times 10^{17}$ for $\sim$ 0.2 micron and at the interface the doping drops with a steepness of 1 decade in $\sim$ 700 Å. Flat active layer profiles and steep interface drop-offs had been obtained previously, but not on the same wafer.

A new growth procedure has been developed as a result of the low active layer growth rate and fast doping response in

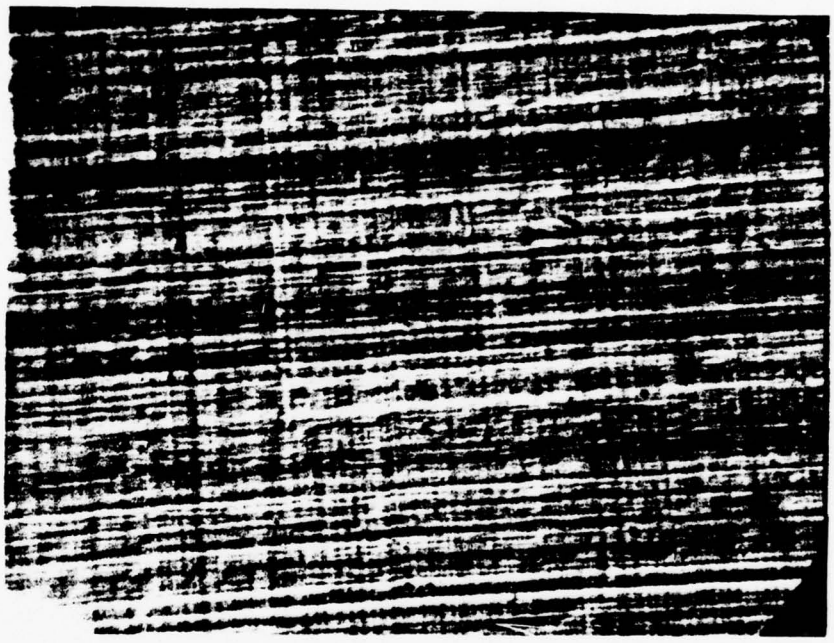


Fig. 19. 15% In surface.

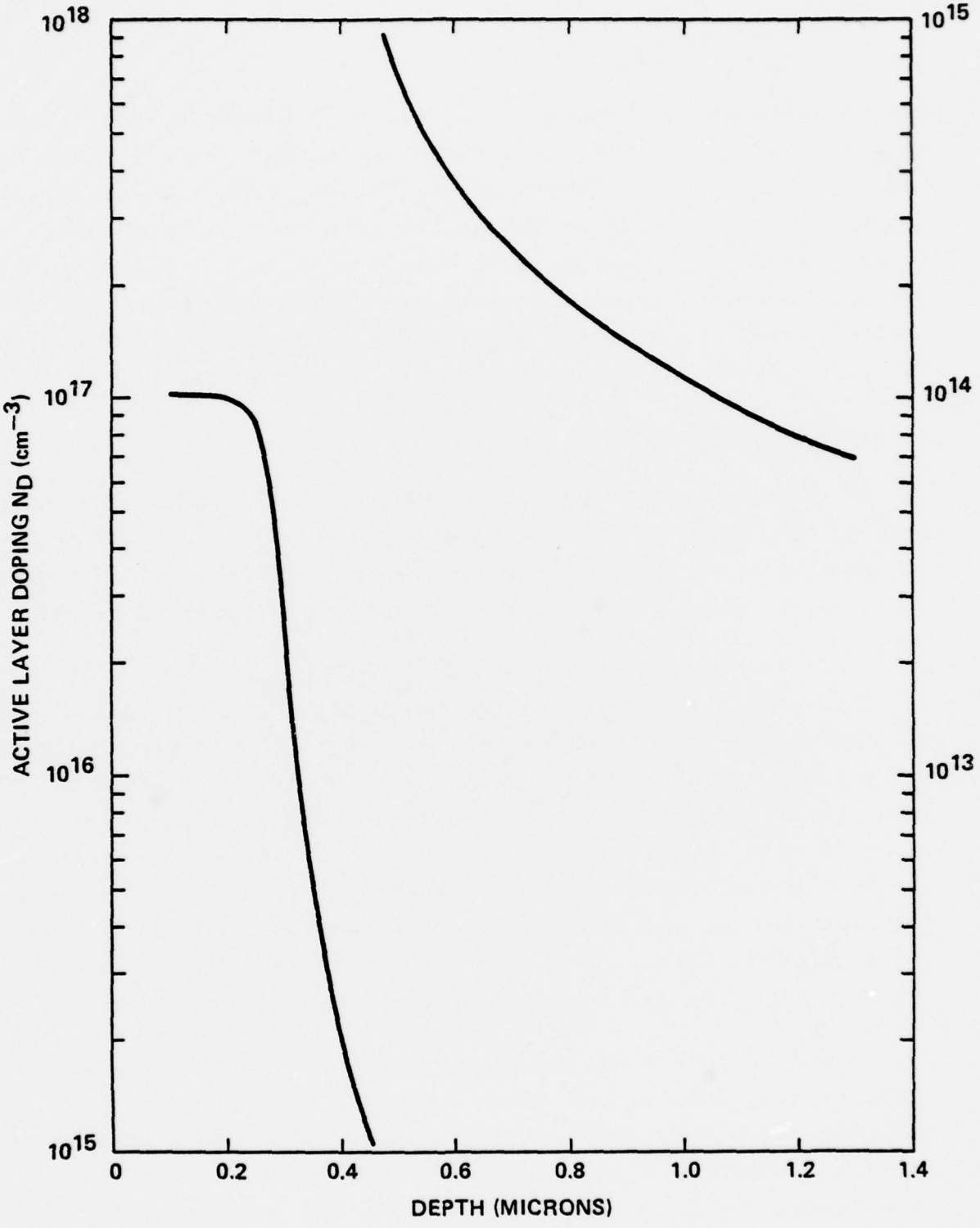


Figure 20. Doping profile for wafer #InG 23-2.

the present reactor system. It basically consists of growing the active layer immediately after the buffer layer with no intermediate vapor etch. Layers grown this way have a grown interface approximately as wide as the growth rate (~ 0.035 micron/min) times the doping response time (2-1/2 min), i.e. 0.1 micron, with no possibility of lattice-mismatch between the active and buffer layers which could degrade FET noise figures. The doping profile of a layer grown this way is shown in Fig. 21.

2.4 Materials Summary

To summarize the development of VPE InGaAs under this contract, the three phases of the development will be briefly reviewed. The earliest work concerned the growth of InGaAs directly on GaAs by using a mixed In/Ga source in a standard GaAs VPE reactor.

The next phase involved the designing, building, and operation of a two-source (InAs,GaAs) reactor. During this period numerous experiments were made to determine the operating conditions of the reactor. Such interactive parameters as the growth rate, grading rate, grading compositions, growth and source temperatures, doping levels, flow rates, and other factors had to be determined. Several reactor modifications were necessary in order to produce progressively better material. Some FET material was produced during this time but reproducibility remained a problem.

The final phase was entered after the two most critical reactor flaws, InAs source crust dissolution and a delay in the doping system response, were corrected. The former problem was solved by the use of sodium-filled heat pipes, and the latter by a redesigned mixing chamber. This greatly enhanced the run-to-run reproducibility and FET quality material began to be produced more consistently. Work then focused on producing material for better FETs. At the close of the contract InGaAs FET material was being regularly produced and its quality was steadily improving. Techniques for further improvements were already under development.

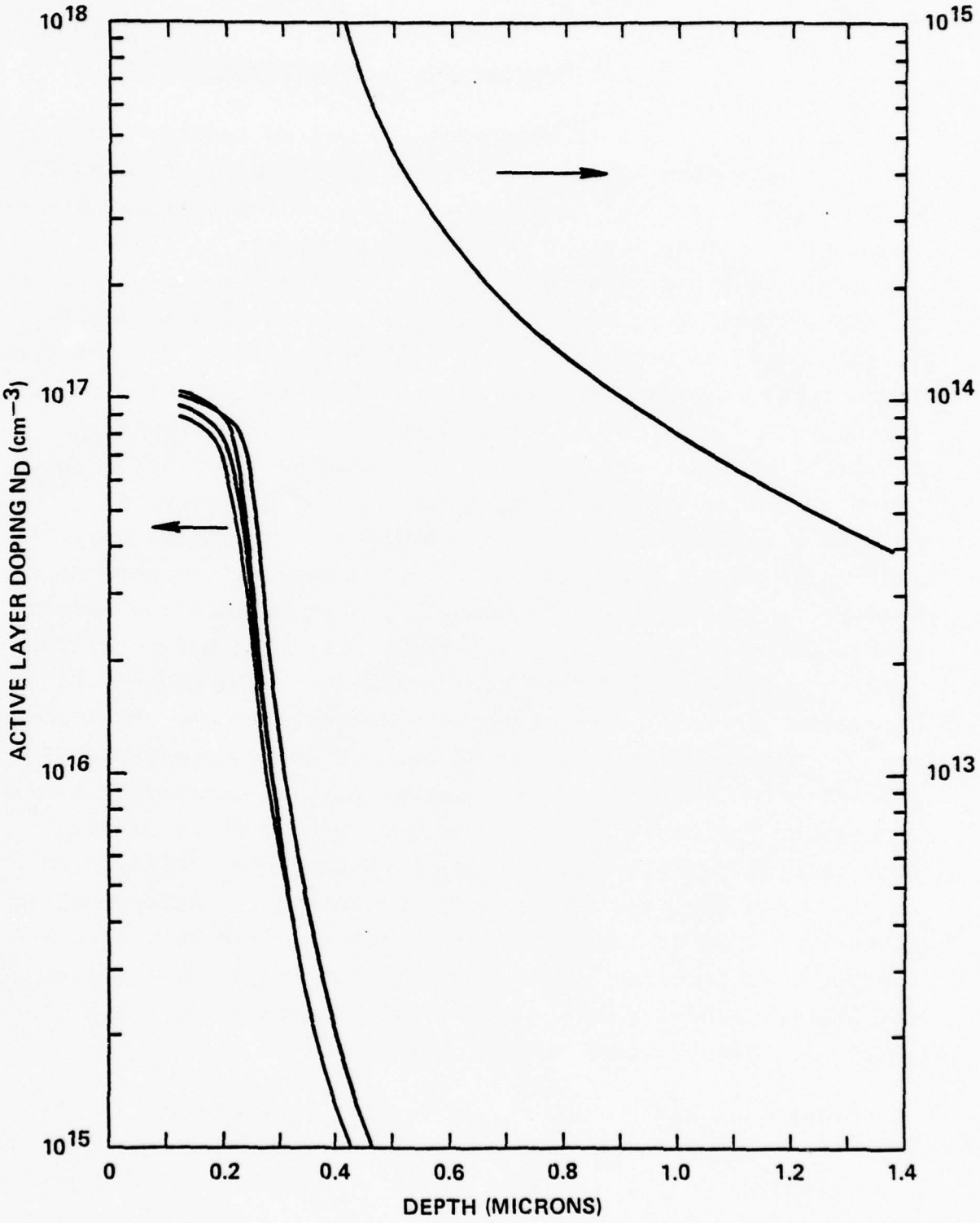


Figure 21. Doping profile for no vapor etch.

3. DEVICE PERFORMANCE CONSIDERATIONS

The ultimate goal of this contract was to ascertain whether or not InGaAs FETs have a significant advantage over GaAs FETs with regard to a lower noise figure (NF) and/or a higher associated gain (G_a) at a given frequency. However, to simply fabricate devices and measure NF and G_a without the measurement of any other indicators would not be too illuminating in determining where the problems lie if such measurements did not yield the desired results. And even if the desired results were obtained, one would want to know to what extent they were the result of a higher effective saturated drift velocity, a lower value of intervalley scattering, or some other parameter. To further complicate matters, no universally acceptable analytical expression exists for NF. An arduous procedure has been developed for calculating NF for GaAs,[36,37] but besides the extreme number of cumbersome steps required, there is a heavy reliance upon empirically determined parameters (e.g. the high-field diffusion constant chosen to give agreement between the theory and the experimental data for NF and the field dependence of the effective electron noise temperature). A relatively simple expression has been developed for the optimum noise figure,[38] but again it contains an empirically determined parameter which is good only for GaAs and unknown for InGaAs. Furthermore, it gives NF = 0 dB if the parasitic source and gate resistances are zero, taking into account none of the noise arising from the intrinsic device such as intervalley scattering noise which has been reported to be important.[39]

Other indicators that can be used to evaluate the InGaAs FETs are the y-parameter data from which the small-signal equivalent circuit can be deduced, the maximum available gain (MAG), and the determination of the effective saturated drift velocity (v_s) in the channel. Specifically however we wish

to answer the following question: for an InGaAs FET having the same geometric parameters, doping, and small-signal equivalent circuit as a GaAs FET (except for the improvements expected from a higher value of v_s which would be reflected in a higher value of MAG) are NF and/or G_a significantly better for the InGaAs FET?

3.1 Effective Saturated Drift Velocity Determination

Although there are various theories describing the drain characteristics of the FET obtained by joining the Shockley gradual channel approximation region near the source end of the channel to a velocity saturated region near the drain end of the channel,[40-42] it will be assumed for this study that the entire channel is velocity saturated everywhere under the gate. It has been found that for the short gate length devices fabricated (around one micron or less) both the transconductance (g_m) and the drain current (I_d) are quite accurately described by the expressions resulting from this assumption, and the resulting analysis will be greatly simplified.

The relationship between this effective saturated drift velocity and the velocity values shown on a velocity-field characteristic is not straightforward because of velocity overshoot,[2,3] as has already been mentioned. Accordingly, v_s will simply afford an empirical basis of comparison between InGaAs and GaAs. For the sake of analysis, it will be assumed that the gate length (L) is short enough so that the electric field is constant throughout the channel at a value above E_s in Fig. 1. Consequently, carrier accumulation and depletion regions are nonexistent[43,44] meaning that the mobile electron charge (n) is equal to the channel doping (N_D) throughout the channel. With v_s and n constant along the channel, the gate depletion depth (w) must also be constant as shown in Fig. 22 to maintain current continuity. For the general case of v_s and N_D varying with x, I_d can thus be written as

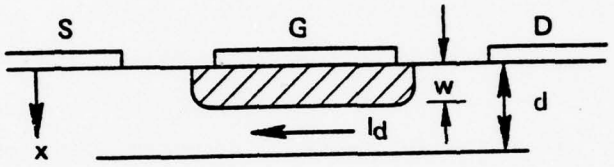


Figure 22. Assumed channel profile.

$$I_d = qZ \int_w^d N_D(x) v_s(x) dx \tag{3-1}$$

where Z is the gate width. Thus with V_g as the gate voltage

$$g_m = \frac{\partial I_d}{\partial V_g} = qZ \frac{\partial}{\partial V_g} \int_w^d N_D(x) v_s(x) dx$$

$$= qZ \left[N_D(d) v_s(d) \frac{\partial d}{\partial V_g} - N_D(w) v_s(w) \frac{\partial w}{\partial V_g} + \int_w^d \frac{\partial (N_D(x) v_s(x))}{\partial V_g} dx \right]$$

$$= - qZ N_D(w) v_s(w) \frac{\partial w}{\partial V_g} \tag{3-2}$$

by application of Leibnitz' rule. An analysis of the gate depletion region assuming that in this region fields along the channel can be neglected gives the following:

$$\frac{\partial^2 V}{\partial x^2} = \frac{q N_D(x)}{\epsilon} \tag{3-3}$$

$$\frac{\partial V}{\partial x} = - \frac{q}{\epsilon} \int N_D(x) dx + A \tag{3-4}$$

$$\frac{\partial V}{\partial x} = 0 \text{ at } x = w, \text{ so } A = \frac{q}{\epsilon} \int N_D(x) dx \Big|_{x=w} \tag{3-5}$$

$$V = - \frac{q}{\epsilon} \iint N_D(x) dx + Ax + B \quad . \tag{3-6}$$

With the assumption that V=0 at x=w to maintain a constant depletion width along the gate length as shown in Fig. 22,

$$B = \frac{q}{\epsilon} \iint N_D(x) dx \Big|_{x=w} - Aw \tag{3-7}$$

and so with a Schottky-barrier gate having a barrier height ϕ_B,

$$V\Big|_{x=0} = V_g - \phi_B = -\frac{q}{\epsilon}\left[\iint N_D(x)dx\Big|_{x=0} - \iint N_D(x)dx\Big|_{x=w} + w\int N_D(x)dx\Big|_{x=w}\right]. \tag{3-8}$$

Differentiation with respect to w gives

$$\frac{\partial V_g}{\partial w} = -\frac{q}{\epsilon}\left[-\int N_D(x)dx\Big|_{x=w} + \int N_D(x)dx\Big|_{x=w} + wN_D(w)\right]$$

$$= -\frac{q}{\epsilon} wN_D(w) \tag{3-9}$$

so Eq. (3-2) becomes

$$g_m = \frac{\epsilon Z v_s(w)}{w} \quad . \tag{3-10}$$

Ignoring the parasitic sidewall fringing capacitance of the gate, the gate capacitance C_{gs} is given by

$$C_{gs} = \frac{\epsilon ZL}{w} \tag{3-11}$$

so that

$$\frac{g_m}{C_{gs}} = \frac{v_s(w)}{L} \quad . \tag{3-12}$$

Another relationship can be developed by differentiating Eq. (3-1) with respect to w and again applying Leibnitz' rule. This simply involves replacing V_g by w in Eq. (3-2), giving

$$\frac{\partial I_d}{\partial w} = -qZN_D(w)v_s(w) \quad . \tag{3-13}$$

If the doping is constant with x, then

$$w = \sqrt{\frac{2\epsilon(\phi_B - V_g)}{qN_D}} \tag{3-14}$$

and Eq. (3-13) becomes

$$\frac{\partial I_d}{\partial(\sqrt{\phi_B - V_g})} = -\sqrt{2\epsilon q N_D}\, Z v_s(w) \quad . \tag{3-15}$$

Equation (3-15) reveals that if I_D is plotted as a function of $\sqrt{\phi_B - V_g}$, the resulting slope will be proportional to v_s so that a profile of v_s across the channel thickness can be obtained in much the same manner as a mobility profile can be obtained.

With N_D constant, Eqs. (3-10) and (3-14) give

$$g_m = \sqrt{\frac{\epsilon q N_D}{2(\phi_B - V_g)}}\, Z v_s(w) \quad . \tag{3-16}$$

If v_s is also constant with channel depth, Eq. (3-1) gives

$$\begin{aligned} I_d &= qZN_D v_s(d-w) \\ &= qZN_D v_s\left(d - \sqrt{\frac{2\epsilon(\phi_B - V_g)}{qN_D}}\right) \\ &= qZN_D d v_s\left(1 - \sqrt{\frac{\phi_B - V_g}{V_p}}\right) \end{aligned} \tag{3-17}$$

where V_p is the channel pinch-off voltage. Equations (3-12), (3-15), and (3-16) all provide means of evaluating v_s from empirical data.

$$v_s = \frac{g_m}{C_{gs}} L \tag{3-18}$$

$$v_s = \frac{-\partial I_D / \partial(\sqrt{\phi_B - V_g})}{Z\sqrt{2\epsilon q N_D}} \tag{3-19}$$

$$v_s = \frac{g_m}{Z}\sqrt{\frac{2(\phi_B - V_g)}{\epsilon q N_D}} \tag{3-20}$$

Although Eqs. (3-19) and (3-20) are not independent, Eq. (3-18) requires the knowledge of C_{gs} and L in place of N_D and ϕ_B. All

three equations evaluate v_s at the gate depletion region edge while Eq. (3-17) would be valid for determining v_s only if v_s did not vary across the channel depth.

3.2 Maximum Available Gain Considerations

Transducer Power Gain (G_T) is defined to be the power delivered by the FET to the load divided by the power that the source alone could deliver to the load if the load were conjugately matched to the source. In terms of the y-parameters of the FET[46]

$$G_T = \frac{4|y_{121}|^2 R_e(Y_L) R_e(Y_S)}{|(y_{11}+Y_S)(y_{22}+Y_L) - y_{12}y_{21}|^2} \tag{3-21}$$

where Y_L and Y_S are the load and source admittances respectively. If the FET is unconditionally stable, G_T may be maximized by conjugately matching the load and source to the FET, giving what is termed the maximum available power gain (MAG) of the FET. Unconditional stability requires[47]

$$K = \frac{2g_{11}g_{22} - R_e(y_{12}y_{21})}{|y_{12}y_{21}|} \geq 1, \quad g_{11}, g_{22} > 0 \tag{3-22}$$

where g_{11} and g_{22} are the real parts of y_{11} and y_{22}. Provided the conditions of Eq. (3-22) are met, then (Ref. 48)

$$MAG = \frac{|y_{21}|^2}{2g_{11}g_{22} - R_e(y_{12}y_{21}) + \sqrt{[2g_{11}g_{22} - R_e(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2}} \tag{3-23}$$

with the following source ($Y_S = G_S + jB_S$) and load ($Y_L = G_L + jB_L$) admittances

$$B_S = -b_{11} + \frac{I_m(y_{12}y_{21})}{2g_{22}} \tag{3-24}$$

$$B_L = -b_{22} + \frac{I_m(y_{12}y_{21})}{2g_{11}} \tag{3-25}$$

$$G_S = \frac{1}{2g_{22}} \sqrt{[2g_{11}g_{22} - R_e(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2} \tag{3-26}$$

$$G_L = \frac{1}{2g_{11}} \sqrt{[2g_{11}g_{22} - R_e(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2} \; . \tag{3-27}$$

3.2.1 Unconditional Stability and Maximum Stable Gain

If the FET is not unconditionally stable (i.e., $K < 1$, which at 8 GHz is characteristic of most of the InGaAs FETs fabricated), then the external lossy admittances G_1 and G_2 shown in Fig. 23 need to be added to bring K up to unity before optimization for Y_S and Y_L takes place. Equations (3-22) and (3-21) thus become

$$K = \frac{2(g_{11}+G_1)(g_{22}+G_2) - R_e(y_{12}y_{21})}{|y_{12}y_{21}|} \tag{3-28}$$

$$MAG = \frac{|y_{21}|^2}{2(g_{11}+G_1)(g_{22}+G_2) - R_e(y_{12}y_{21}) + \sqrt{[2(g_{11}+G_1)(g_{22}+G_2) - R_e(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2}} \tag{3-29}$$

These two equations can be combined to give

$$MAG = \left| \frac{y_{21}}{y_{12}} \right| \frac{1}{K + \sqrt{K^2-1}} \tag{3-30}$$

which reveals that G_1 and G_2 should bring K back to unity but not more, lest MAG be reduced. Since G_1 and G_2 always increase

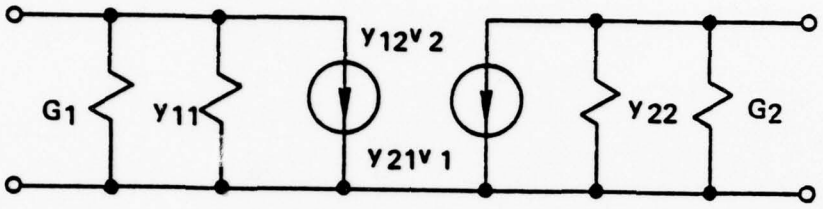


Figure 23. Y-parameter model with lossy admittances G_1 and G_2 added for stability.

K in the positive direction, if $K \geq 1$ for the FET by itself, then $G_1 = G_2 = 0$. Thus, if $K < 1$ for the FET by itself, G_1 and G_2 must be added such that $K = 1$ in Eq. (3-28). This gives a relationship for determining G_1 and G_2

$$\frac{2(g_{11}+G_1)(g_{22}+G_2) - R_e(y_{12}y_{21})}{|y_{12}y_{21}|} = 1 \quad , \tag{3-31}$$

however it is not a unique determination. For $G_2 = 0$,

$$G_1 = \frac{|y_{12}y_{21}| + R_e(y_{12}y_{21})}{2g_{22}} - g_{11} \tag{3-32}$$

while for $G_1 = 0$,

$$G_2 = \frac{|y_{12}y_{21}| + R_e(y_{12}y_{21})}{2g_{11}} - g_{22} \tag{3-33}$$

and finally for $G_1 = G_2$,

$$G_1 = G_2 = -\frac{(g_{11}+g_{22})}{2} + \frac{1}{2}\sqrt{(g_{11}-g_{22})^2 + 2\left[|y_{12}y_{21}| + R_e(y_{12}y_{21})\right]} \; . \tag{3-34}$$

However G_1 and G_2 are chosen, $K = 1$ and Eq. (3-30) reduces to what is termed the maximum stable gain MSG

$$MSG = \left|\frac{y_{21}}{y_{12}}\right| \; . \tag{3-35}$$

With the addition of G_1 and G_2 to achieve unconditional stability, Eqs. (3-24) through (3-27) for the optimum source and load admittances are modified by replacing g_{11} by $g_{11}+G_1$ and g_{22} by $g_{22}+G_2$.

3.2.2 Gain Maximization Through Feedback Control

So far the power gain considerations have dealt with optimizing the gain by the use of optimum source and load admittances. But what if the FET y-parameters themselves can be optimized? One of the hopes for InGaAs is to realize a higher effective saturated drift velocity which in turn will increase g_m and hence y_{21} over that for GaAs, resulting in a higher value of MAG by Eq. (3-23). Suppose that g_{11} and g_{22} are also each fixed at some particular value. The only remaining parameter in Eq. (3-23) is y_{12}. What is the desired value of y_{12} to maximize MAG? Do the parasitics (source resistance R_s, source inductance L_s and gate-to-drain feedback capacitance C_{gd}) that prevent the feedback parameter y_{12} from being zero help or hurt in realizing the highest possible value of MAG? If R_s, L_s and C_{gd} are zero, the $y_{12} = 0$ and Eq. (3-23) gives

$$MAG = \frac{|y_{21}|^2}{4g_{11}g_{22}} \tag{3-36}$$

But is $y_{12} = 0$ really optimum?

First of all, if g_{11} or g_{22} is negative, then the criterion for stability (Eq. (3-22)) has been violated, so it will be assumed that g_{11} and g_{22} are both positive. If $2g_{11}g_{22} \leq R_e(y_{12}y_{21})$, then instability also results since $2g_{11}g_{22} > 0$ and by Eq. (3-22) $K \leq 0$. If indeed $2g_{11}g_{22} \leq R_e(y_{12}y_{21})$, G_1 and G_2 must be added as previously discussed, so it will be assumed in the following that g_{11} and g_{22} include the effects of G_1 and G_2 so as to give unconditional stability.

With $2g_{11}g_{22}-R_e(y_{12}y_{21}) > 0$, Eq. (3-23) reveals that MAG will be maximized if the variable y_{12} is chosen so as to minimize $2g_{11}g_{22}-R_e(y_{12}y_{21})$ subject to the constraint that $2g_{11}g_{22}-R_e(y_{12}y_{21})$ cannot be less than $|y_{12}y_{21}|$ to maintain unconditional stability.

Thus y_{12} should be chosen so as to minimize the equation

$$2g_{11}g_{22} - R_e(y_{12}y_{21}) = |y_{12}y_{21}| \tag{3-37}$$

which corresponds to K = 1. With the identification

$$R_e(y_{12}y_{21}) = A = g_{21}g_{12} - b_{21}b_{12} \tag{3-38}$$

$$I_m(y_{12}y_{21}) = B = g_{21}b_{12} + g_{12}b_{21} \tag{3-39}$$

then Eq. (3-37) becomes

$$2g_{11}g_{22} - A = \sqrt{A^2+B^2} \tag{3-40}$$

which is obviously minimum with

$$B = 0 \tag{3-41}$$

$$A = g_{11}g_{22} \tag{3-42}$$

giving

$$MAG_{max} = \frac{|y_{21}|^2}{g_{11}g_{22}} \tag{3-43}$$

which is 6 dB better than the value given in Eq. (3-36) where $y_{12} = 0$. Thus the proper choice of the values of the parasitic elements R_s, L_s, and C_{gd} can be used to achieve up to 6 dB improvement in MAG from what it would be if the parasitic elements were absent. Equations (3-38), (3-39), (3-41), and (3-42) can be solved simultaneously to yield the optimum values for g_{12} and b_{12}.

$$g_{12}|_{opt} = g_{21}\frac{g_{11}g_{22}}{|y_{21}|^2} \tag{3-44}$$

$$b_{12}|_{opt} = -b_{21}\frac{g_{11}g_{22}}{|y_{21}|^2} \tag{3-45}$$

Although it may be difficult to achieve such optimum values for g_{12} and b_{12} in practice in addition to the fact that they cannot be varied without affecting the other y-parameters, this analysis does reveal the important role that feedback plays in achieving high values of MAG. To simple-mindedly strive for a high value of v_s by going to InGaAs and at the same time to make an effort to cut the parasitics to zero could be a goal that, even if successfully achieved could result in FET performance perhaps inferior to that achieved with GaAs.

3.3 Small-Signal Equivalent Circuit Model

The equivalent circuit shown in Fig. 24 is typical of the earlier models used for the FET.[49] This model predicts

$$\frac{g_{11}}{b_{11}} = \frac{-b_{21}}{g_{21}} = \omega C_{gs}(r_c+R_g+R_s)/(1+g_m R_s) \qquad (3\text{-}46)$$

while for the InGaAs FETs fabricated (and also for GaAs FETs),

$$\frac{-b_{21}}{g_{21}} \approx f\,\frac{g_{11}}{b_{11}} \qquad (3\text{-}47)$$

where f is a numerical factor that ranges from 2-3 as shown in Table V.

TABLE V

FET No.	f	FET No.	f
GaAs 38-4 (Ref.50)	3.34	InGaAs 58-6	3.23
InGaAs 45-3	2.52	InGaAs 59-1	1.54
InGaAs 45-11	3.12	InGaAs 61-1	3.1
InGaAs 53-11	2.18	InGaAs 61-2	2.75
InGaAs 58-3	1.55	InGaAs 61-3	3.29

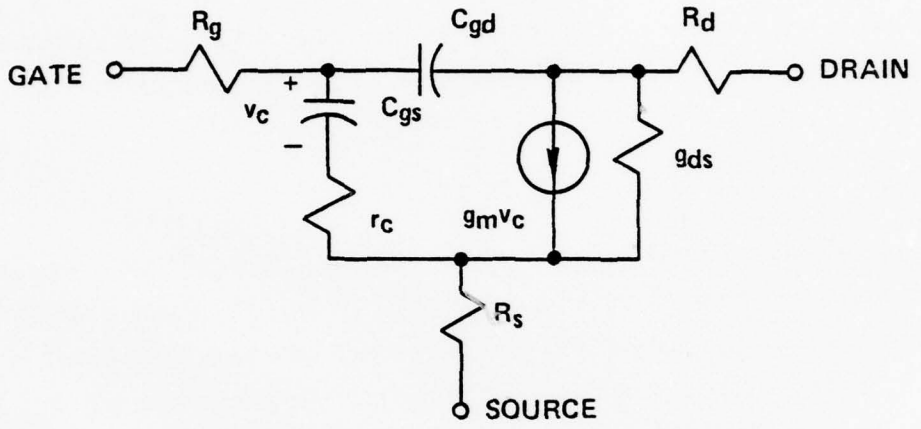


Figure 24. Early small-signal FET model.

Later models[51-53] get around this problem by introducing a phase factor to g_m,

$$g_m = g_{mo} e^{-i\omega\tau_o} \tag{3-48}$$

which basically increases b_{21} by adding τ_o to $r_c C_{gs}$. The physical meaning given to τ_o is that it is the delay corresponding to the time required to traverse the gate length at a velocity, v_s, or

$$\tau_o \sim \frac{L}{v_s} \tag{3-49}$$

It appears however that this would not be an accurate way of determining v_s since data are given[52,53] which show a 2:1 variation in τ_o for a number of devices all having the same gate length. It is stated that the frequency dependence of g_m as given by Eq. (3-48) is the result of the RC-transmission line character of the FET. It would be better to actually distribute the gate than to lump this effect into g_m in order to remain as close to the physical situation as possible. A correct model for the input impedance of the FET is important, especially in determining the noise figure of the device.[38]

With the assumption of a uniformly depleted channel as shown in Fig. 22, the gate-to-source impedance Z is given by[54]

$$Z = \frac{R}{\Gamma \tanh \Gamma} \tag{3-50}$$

$$\Gamma^2 = j\omega RC \quad , \tag{3-51}$$

where R and C are the total channel resistance and gate capacitance, respectively. For $RC \ll 1$,

$$Y_{11} = \frac{1}{R} \Gamma \tanh \Gamma \cong j\omega C + \frac{\omega^2 R^2 C^2}{3} \tag{3-52}$$

which is modelled by Fig 25. If the total channel resistance is

kept the same, then $r_c = R$ and with $C = C_{gs}$, Eq. (3-52) gives

$$C_2 = C_{gs}/\sqrt{3} = 0.577\ C_{gs} \tag{3-53}$$

$$C_1 = 0.423\ C_{gs} \quad . \tag{3-54}$$

There are still only two unknowns (r_c and C_{gs}) in contrast to three unknowns (r_c, C_{gs}, and τ_o) when Eq. (3-48) is used. The model of Fig. 25 gives

$$\frac{-b_{21}}{g_{21}} = \sqrt{3}\ \frac{g_{11}}{b_{11}} \tag{3-55}$$

which results in values of f still a little below those given in Table V. The assumption of an input parasitic capacitance can account for the remaining difference.

The addition of a capacitance C_o across g_{ds} is needed to give $g_{12} > 0$.[55]

It has been found that below about 6 GHz the gate and drain bond lead inductances (L_g and L_d) can be ignored, but the source bond lead inductance (L_s) cannot. This is because

$$b_{21} \simeq -\omega g_m (r_c C_2 + g_m L_s) \tag{3-56}$$

so that L_s enters to the same degree no matter how low the frequency is. For device #53-11, for example, $r_c C_2 = 8 \times 10^{-12}$ and $g_m L_s = 5.8 \times 10^{-12}$, clearly demonstrating the importance of including L_s in the model no matter what the frequency range of interest is.

Another feature of the empirical data is that b_{12} goes th through zero at around 8 GHz and becomes positive at frequencies above this. Introducing a resistance r_f in series with C_{gd} into the small signal model as some have done [52,53] can model this behavior for b_{12}. However the values of r_f are rather high,

Figure 25. Two-lump model of gate.

ranging from 200 to 2000 ohms,[52,53] and for device #53-11 r_f needs to be 1100 ohms to achieve $b_{12} = 0$ at the correct frequency. Such large values for r_f do not seem to have any basis in reality. As suggested by Fig. 26, it would seem that

$$\frac{r_f}{r_c} \sim \frac{C_{gd}}{C_{gs}} \tag{3-57}$$

and hence that r_f would be much less than r_c to the point of being negligible. A good physical argument for r_f could not be given other than it is needed in the model to fit the empirical data.[56]

It has been found that by returning the input and output parasitic capacitances (C_3 and C_4) to the node between L_s and R_s as shown in Fig. 27, the zero crossing of b_{12} at ~ 8 GHz can be accounted for. As discussed previously, C_3 is also needed to account for the slightly higher empirical values for f than given by Eq. (3-55). Evidently L_g and L_d are not involved in the zero crossing of b_{12} since x_{12} (the imaginary part of the z-parameter z_{12}) is independent of L_g and L_d, and yet it undergoes a zero crossing at nearly the same frequency as b_{12}. Ignoring g_m, r_c, R_s, and g_{ds}, the value of L_s needed to give the zero crossing at a radian frequency of ω is given by

$$\frac{1}{\omega^2 L_s} = \frac{(C_o+C_4)(C_{gs}+C_3)}{C_{gd}} + C_o+C_{gs}+C_3+C_4 \tag{3-58}$$

which shows that C_{gd} causes a capacitance amplification to occur since typically C_{gd} is less than either of C_o or C_3. This in turn causes an LC resonance to occur at much lower frequencies than would ordinarily be expected from considering the resonating capacitance as simply the sum of all the capacitances.

Figure 28 shows the small-signal equivalent circuit model when all the previously discussed considerations are incorporated into the model of Fig. 24.

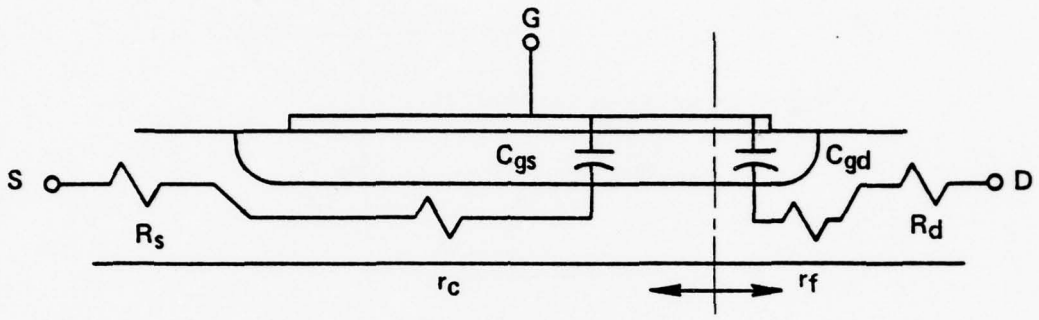


Figure 26. Model for estimating r_f magnitude.

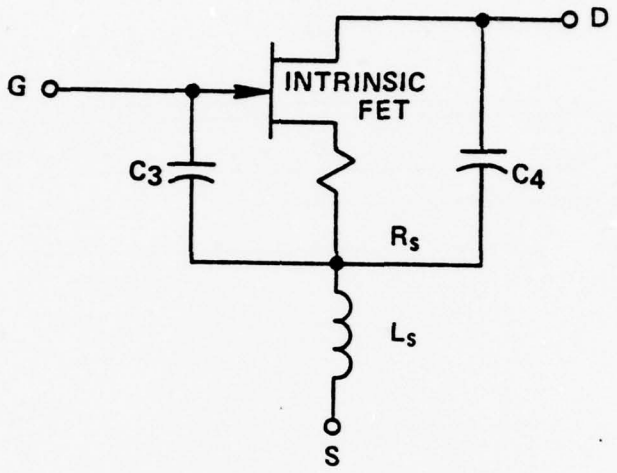


Figure 27. Extrinsic parasitics for FET.

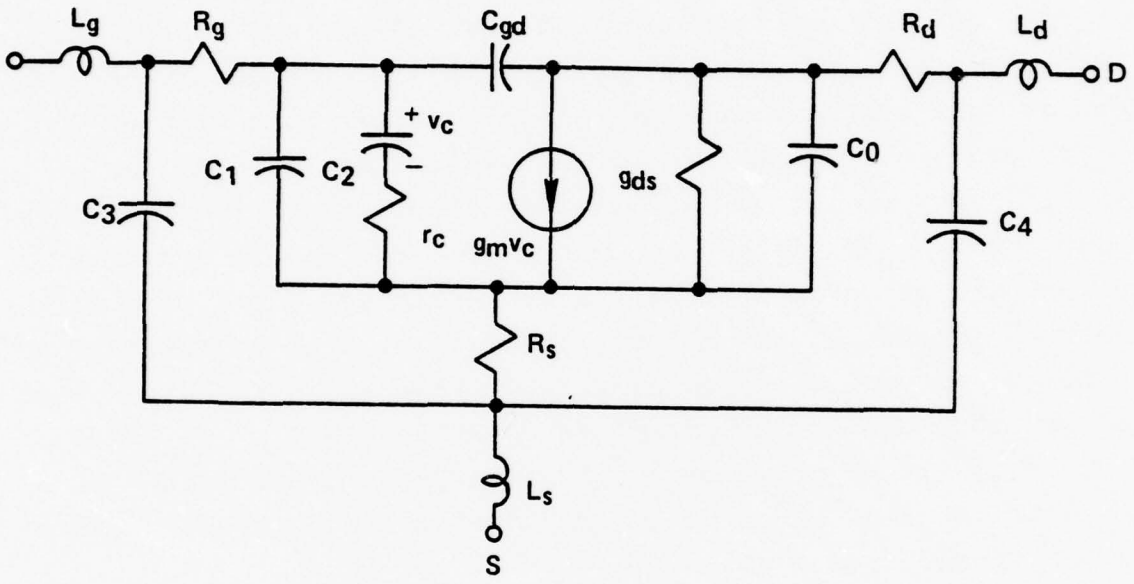


Figure 28. Full small-signal equivalent circuit model.

It has been found that the y-parameter data are described in the 2-6 GHz range by g_{21} and g_{22} being constant; b_{11}, b_{21}, b_{12}, and b_{22} varying 3 dB/octave; and g_{11} and g_{12} varying 6 dB/octave. Along with the zero crossing of x_{12}, this will result in nine equations which will determine nine of the 15 parameters in Fig. 28. With the y-parameters following slopes of 0, 3, and 6 dB/octave, L_g and L_d can be neglected. C_1 and C_2 together form only one unknown by the use of Eqs. (3-53) and (3-54). R_s can be determined at dc by forward biasing the gate with a known current and measuring the floating drain bias with an electrometer. R_d can be measured in a similar way. R_g is typically very small and is virtually impossible to measure for a particular device either at dc or by extracting it from the y-parameters since it is essentially in series with r_c and difficult to separate out. For the purposes of this investigation it will be assumed to be negligible. Since R_d is much less than the magnitude of the impedances associated with C_{gd}, g_{ds}, and C_o, it too will be neglected in the analysis. This leaves nine remaining unknowns to be determined from the eight y-parameters and the frequency for which $x_{12} = 0$.

The attainment of good y-parameter data was considered the weakest link in obtaining numerical values for the model of Fig. 28 for any particular InGaAs FET. The y-parameters were derived from s-parameter measurements taken with Hewlett Packard 8542B Automatic Network Analyzers located both at Varian and at Western Automatic Test Systems (WATS) in Sunnyvale, CA. Not only would the data frequently exhibit waviness, but for the same device different results were obtained from each analyzer and different results were obtained on the same analyzer at different times. For example, for one run of devices good y_{21},y_{12} but poor y_{11},y_{22} data were obtained from the Varian analyzer while good y_{11},y_{22} but poor y_{21},y_{12} data were obtained from the WATS analyzer. Testing has been done using a

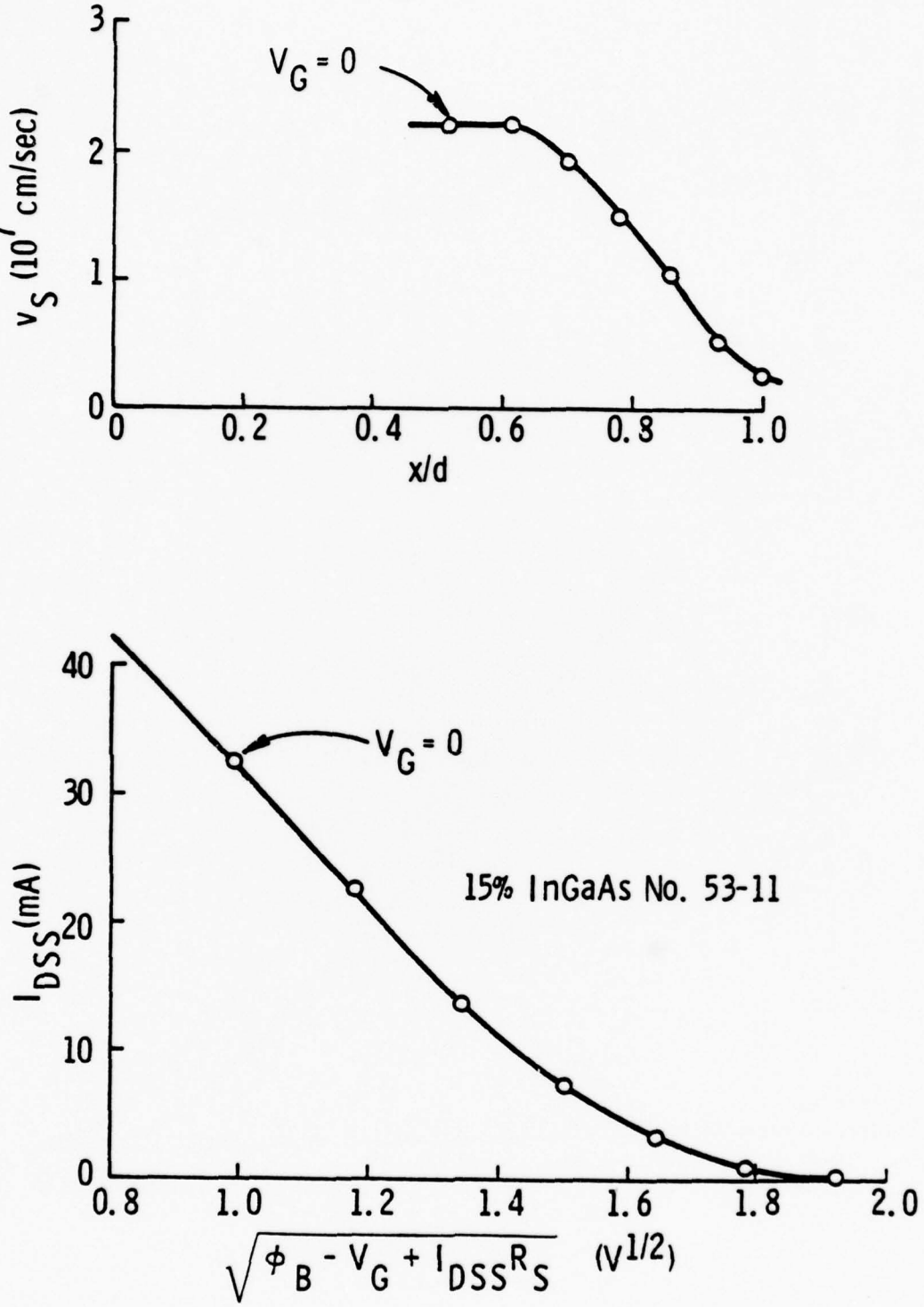


Fig. 29. (Lower) Pinch-off characteristic of an InGaAs FET, and (upper) the "saturated velocity profile" deduced from this.

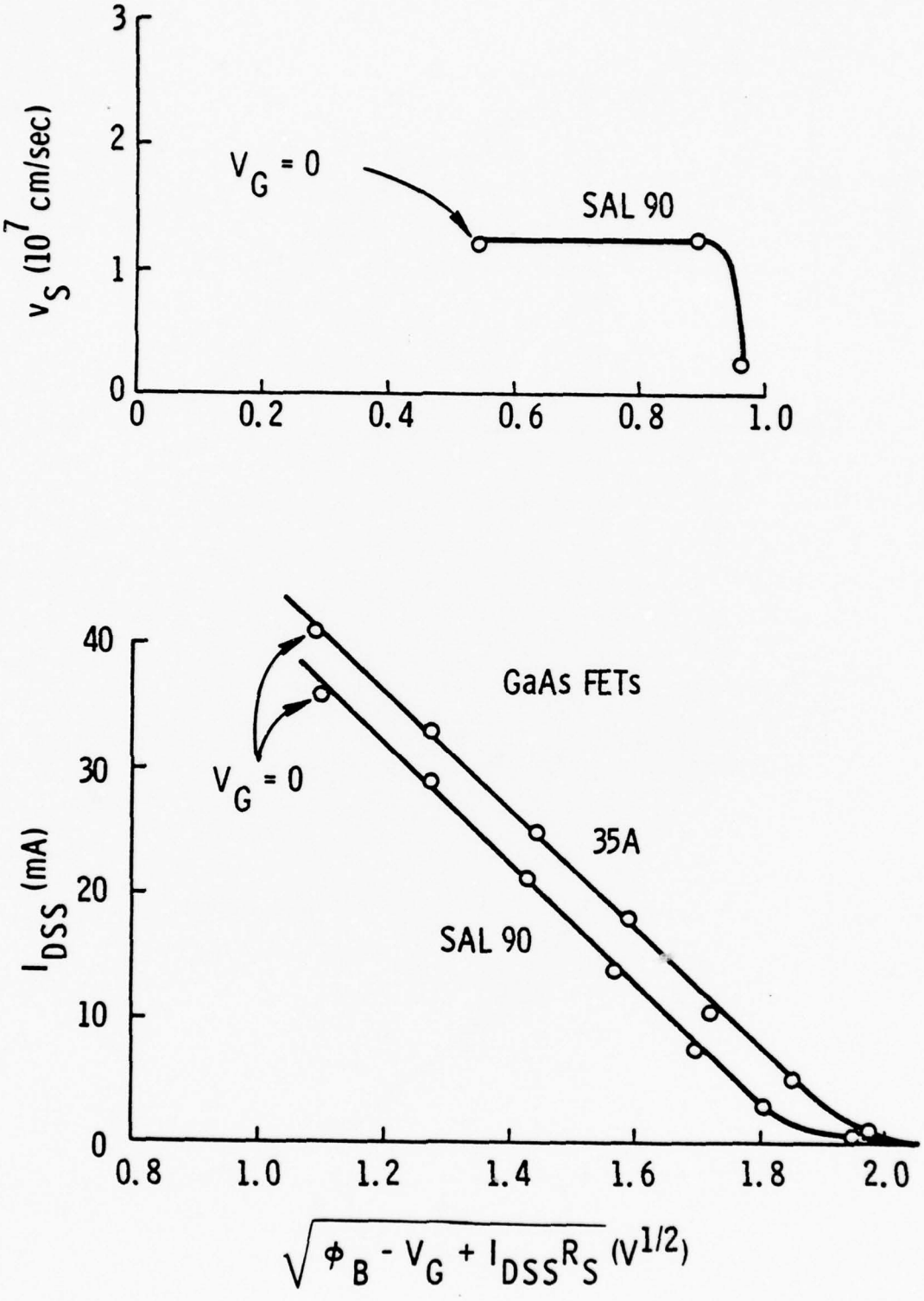


Fig. 30. Pinch-off characteristic and saturated velocity profile for a GaAs FET.

degrading much further away from the active layer-buffer layer interface than it does from the active layer-substrate interface (no buffer layer) of the GaAs FETs. The linearity of the I_d plot for GaAs gives credence to the validity of Eqs. (3-15) and (3-19). It is shown in Appendix A that the 'tail' in the I_d vs $\phi_B - V_g + I_d R_s$ plot is not due to the falloff in the doping N_D, and Appendix B shows that it is not due to the device falling out of complete velocity saturation as pinch-off is approached. Figures 31 and 32 show the predicted[58] NF behavior of the GaAs and InGaAs FETs for v_s constant across the channel and also for the InGaAs FET having the degraded v_s profile shown in Fig. 29. These results clearly show the importance of solving the problem of v_s degradation at the interface.

To get a qualitative feel for the dependency of NF on v_s, assume the simple noise model as shown in Fig. 33, where gate noise and its correlation with the drain noise and noise due to extrinsic elements have been disregarded. The optimum noise figure for this model is

$$NF = 1 + \left(\frac{\omega C_{gs}}{g_m}\right)^2 \frac{\bar{i}_n^2 r_c}{3kTB} \quad . \tag{3-59}$$

Using the simple Drude model,[59] the thermal noise current generated by a completely velocity-saturated resistor for fields greater than E_s (Fig. 1) is

$$\bar{i}_n^2 = \frac{4kTB}{R}\left(\frac{E_s}{\bar{E}}\right) \tag{3-60}$$

where R is the low-field resistance. Assuming this to be the only source of noise, Eq. (3-59) becomes

$$NF = 1 + \left(\frac{4}{3}\right)\left(\frac{\omega C_{gs}}{g_m}\right)^2 \left(\frac{r_c}{R}\right)\left(\frac{T_e}{T_s}\right)\left(\frac{E_s}{\bar{E}}\right) \tag{3-61}$$

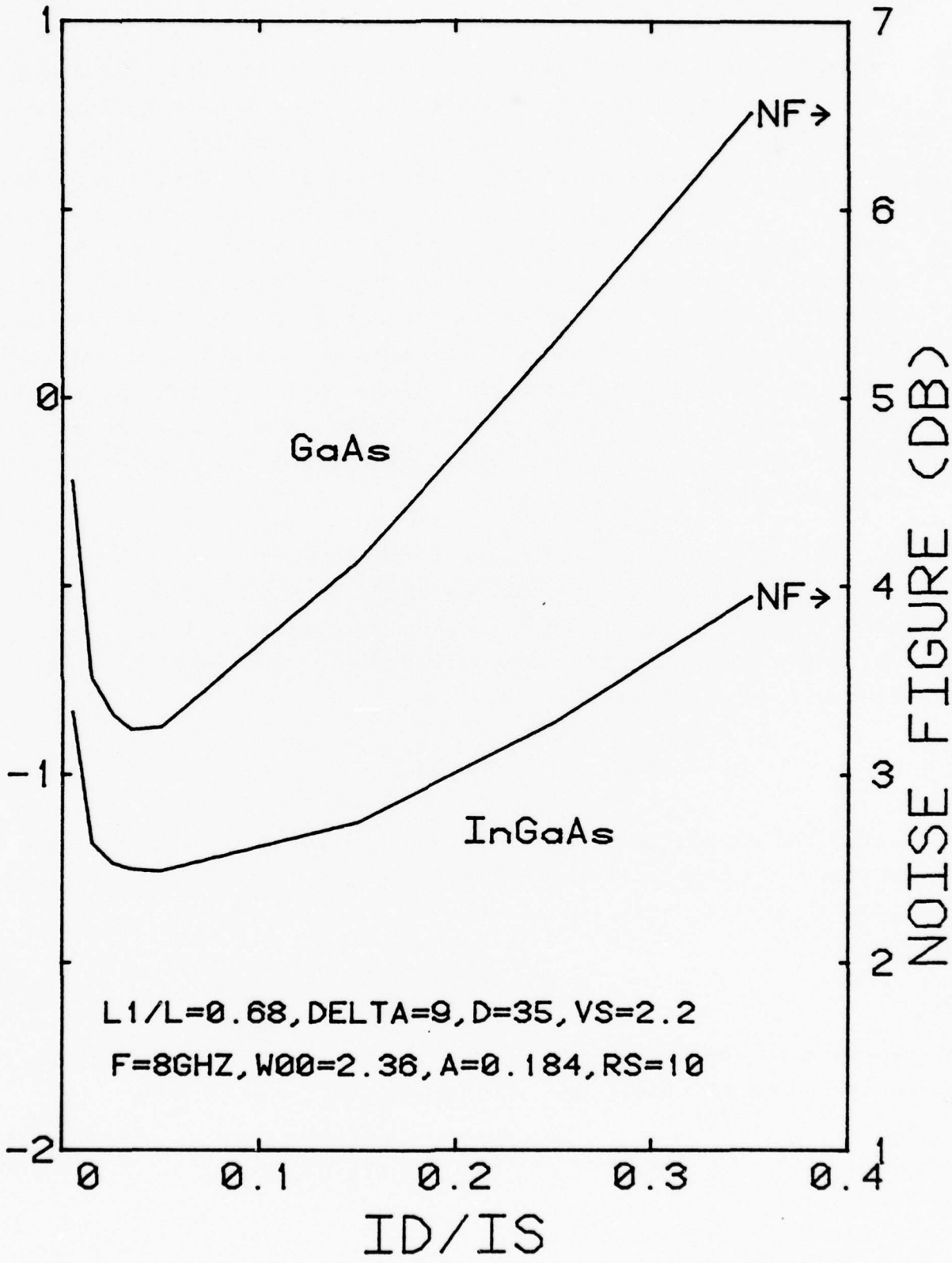


Fig. 31. Predicted behavior of GaAs and InGaAs FETs (15% InAs) with uniform saturated velocity profiles.

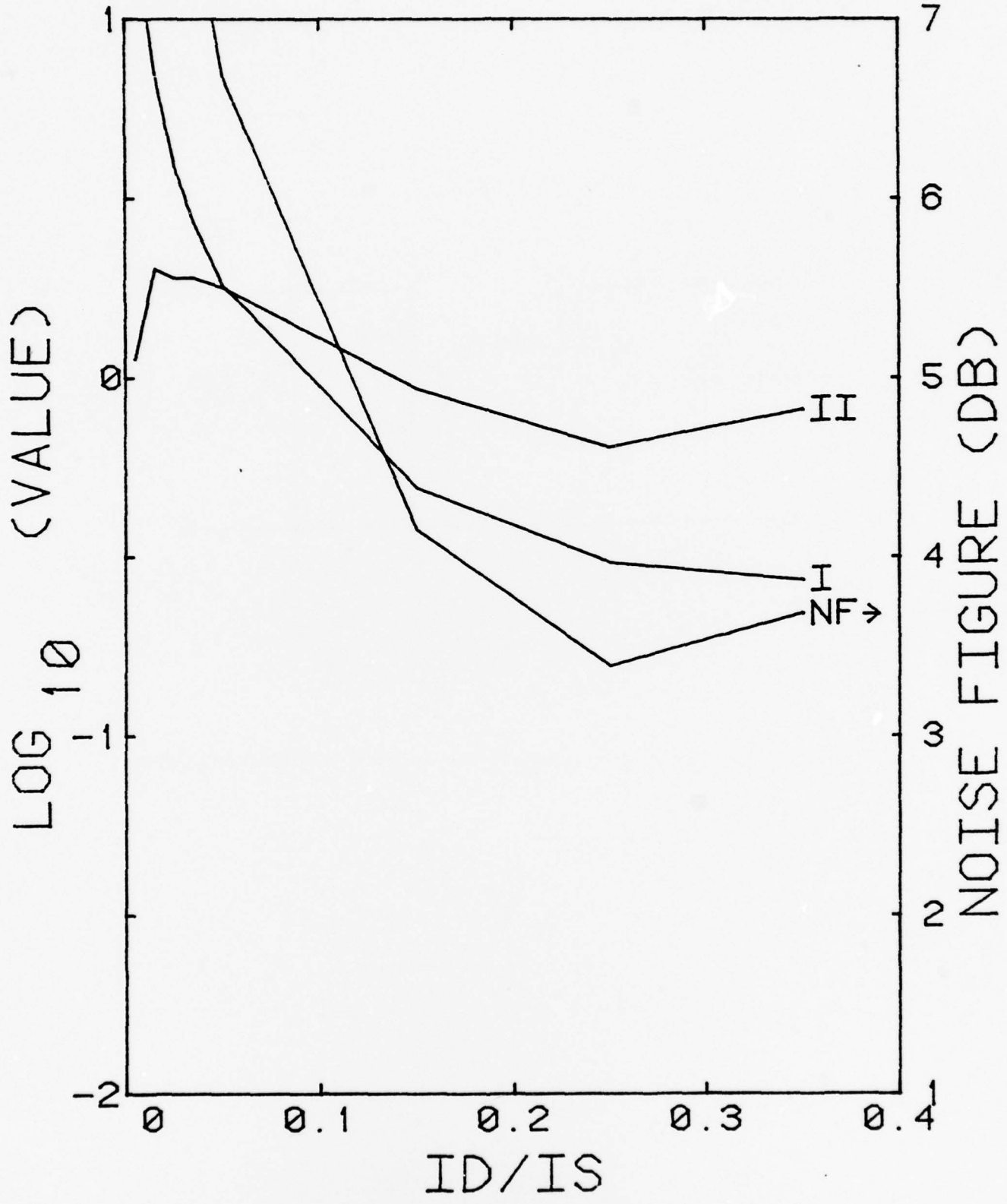


Fig. 32. Results of the computer model using the velocity profile of Fig. 29.

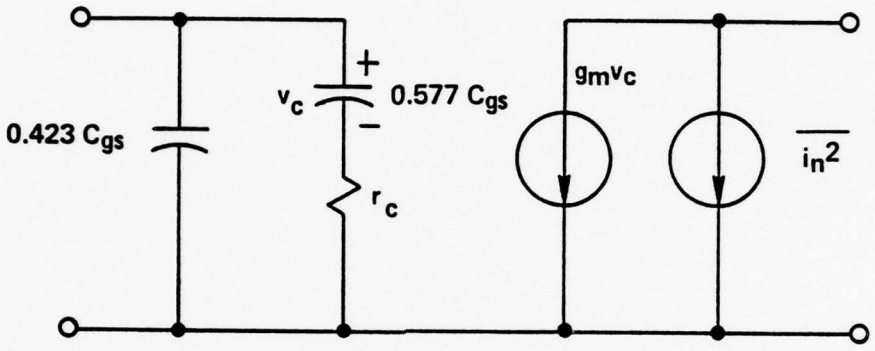


Figure 33. Simple noise model with distributed gate.

where T_e is the electron temperature and T_S is the source temperature. Using Eqs. (3-10) and (3-11) and with

$$r_c \cong g_m^{-1} \tag{3-62}$$

$$R \propto \left(1-\frac{w}{d}\right) \quad , \tag{3-63}$$

then

$$NF = 1 + C \frac{\left(1-\frac{w}{d}\right)\left(\frac{w}{d}\right)}{v_s^3} \quad . \tag{3-64}$$

Setting C to give NF = 3.5 dB at $V_g = 0$ as obtained for one of the better InGaAs devices of run #53 and using the v_s profile shown in Fig. 29 results in the NF plot shown in Fig. 34. Also shown for comparison purposes is the NF plot for GaAs using the v_s profile of Fig. 30 and using the same value of C except that it is scaled to account for the different value of L (C is proportional to L). This clearly demonstrates how the v_s profile can affect the bias for minimum noise figure.

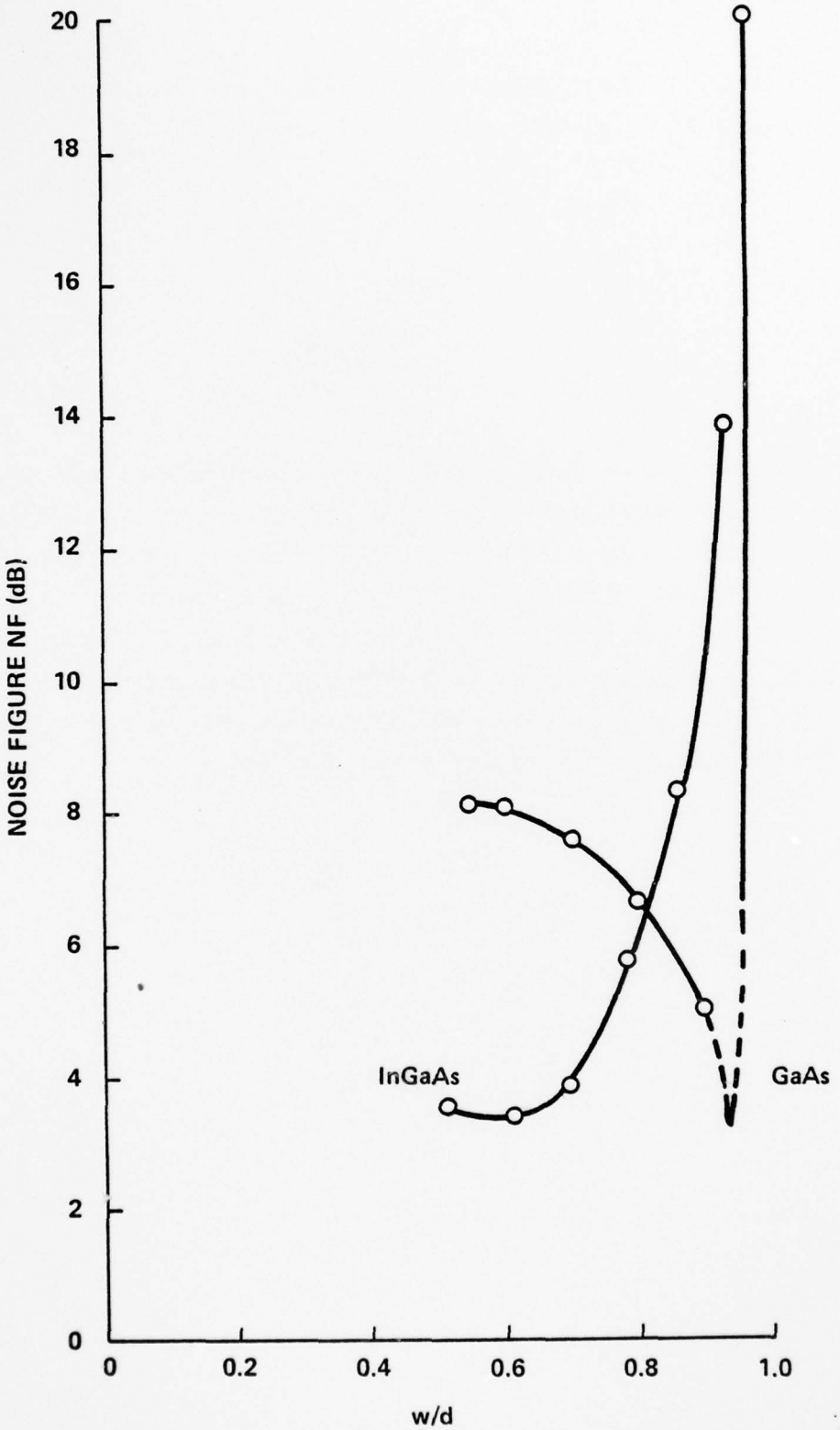


Figure 34. Noise figure bias dependence qualitatively illustrating the effect of interface velocity degradation.

4. DEVICE FABRICATION AND EVALUATION

Since device performance limitations were tied quite closely to the development of the materials technology, the device performance results will be chronicled under headings denoting the different stages of reactor development.

All of the device runs before run #56 used the device geometry shown in Fig. 35 while runs #56 and later used the device geometry shown in Fig. 36. The gate widths are Z = 200 microns for Fig. 35 and Z ≈ 150 microns for Fig. 36. The Fig. 36 geometry permitted electron beam writing of the gates by a single sweep of the beam. Smaller gate lengths were attainable by electron beam exposure, and with the shorter gate lengths the Z dimension is reduced to keep the gate resistance low. Both device geometries had been previously used for GaAs FET fabrication and were not developed specifically for the InGaAs FETs.

The same Au-Ge/Ni ohmic contacts used for GaAs FETs[60] were used for all of the InGaAs FETs fabricated with the feeling that with the smaller barrier height[61] specific contact resistance should be lower for the InGaAs FETs. As will be seen for runs #58 and 59, the source resistance was mainly due to the source-gate spacing and not the specific contact resistance of the metallization. The Schottky-barrier gates were 1000-Å sputtered Pt overlaid with 2000-3000 Å of Au. Both Al and Pt have been used as gates on GaAs FETs at Varian, but because Pt has around a 0.1 eV higher barrier height than Al[62] and since, as the In percentage increases, the barrier height becomes smaller, Pt was used. The fabrication sequence in order was: mesa etch, ohmic contact formation, gate deposition, and Au overlay.

All s-parameter measurements were made with the device die bonded directly onto a microstrip fixture. Prior to run #56 the power gain and noise figure measurements were made using

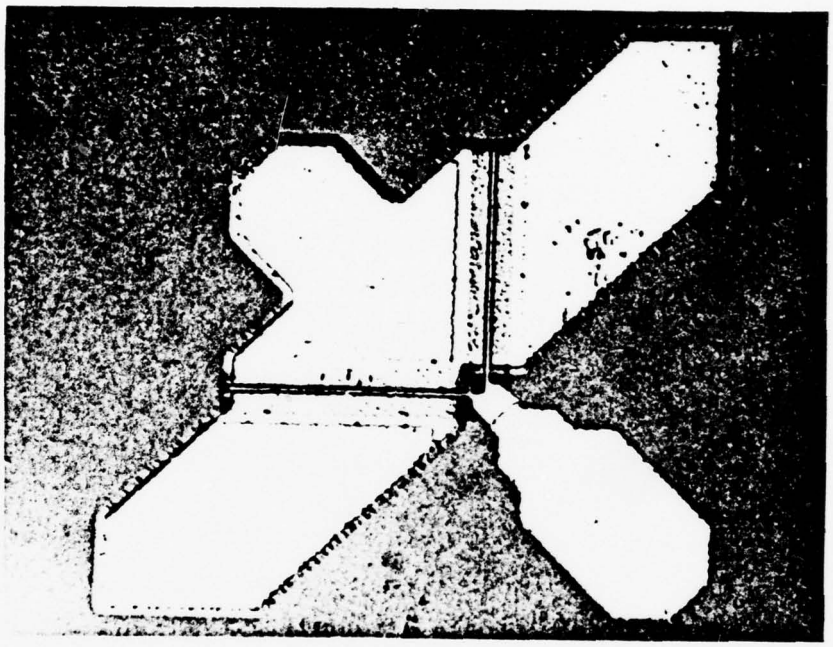


Fig. 35. Device geometry used for runs prior to run #56.

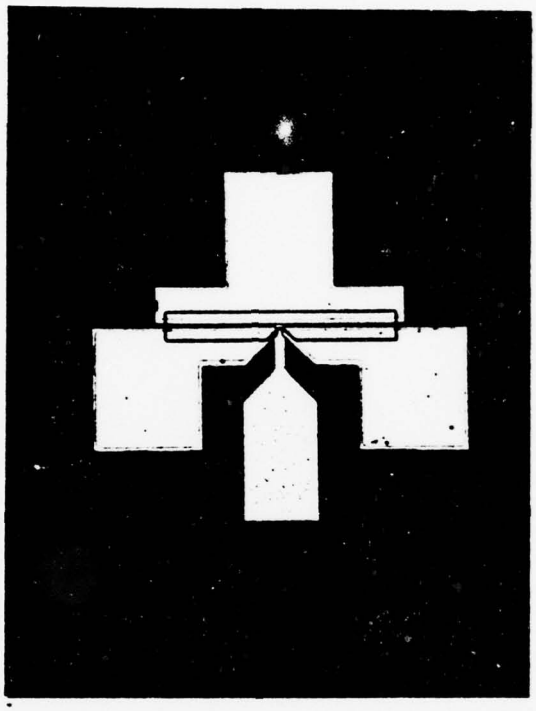


Fig. 36. Device geometry used for run #56 and later.

the same fixture. For runs #56 and later a tunable microstrip amplifier was used for the gain and noise measurements. Initially some of the devices were bonded into Kyocera's ML-7 package and then tested in a microstrip jig for gain and noise. These test fixtures were previously used for testing GaAs FETs and were not developed specifically for the InGaAs FETs.

4.1 Mixed-Source System

All the active layers grown in this system were, of course, grown directly on GaAs Cr-doped substrates without an intervening buffer layer.

4.1.1 Run #38 (3.8% In)

The gate lengths for these devices ranged from 1.3 to 1.6 microns and the channel doping was 7-8 x 10^{16} cm^{-3} as shown by the profile in Appendix C. Y-parameter data for several of the devices are shown in Appendix D and the results at 8 GHz are shown in Table VI. Y-parameter measurements on the best GaAs FETs (run #35A) at that time using the same Fig. 35 geometry and having the same 1.3 to 1.6 micron gate lengths are also included in Appendix D and shown in Table VI.

TABLE VI: Y-Parameter Performance for Run #38

Device #	Power Gain at 8 GHz (dB)	g_{22} (mmho)
38 - 2	13.2 (MSG)	1.0
38 - 3	14.1 (MSG)	0.5
38 -16	12.2 (MSG)	0.62
38 -31	14.4 (MSG)	0.65
35A-12	16.5 (MAG)	1.1
35A-16	13.5 (MAG)	1.69

Actual power gain measurements are given in Table VII.

TABLE VII: 7-GHz Performance for Run #38

Device #	MAG (dB)	Minimum Noise Figure NF_m (dB)	Associated Gain G_a (dB)
38-2	11.5	6.72	5.4
35A-12	12.9	---	---

The InGaAs and GaAs power gains are comparable, but the output conductance g_{22} appears generally to be around a factor of two lower for the InGaAs devices. Heterojunction confinement which occurs as the result of the step in bandgap at the InGaAs-GaAs interface[63] acts to help constrain the electrons to the epitaxial (InGaAs) layer and prevent penetration of hot electrons into the substrate at the pinch-off region where they flow as a space-charge-limited current. Since a significant contribution to the output conductance arises from electrons that travel around the pinch-off region via the substrate[64-66] the heterojunction confinement reduces the output conductance. This reduction in g_{22} causes the stability factor K to be less than unity and is why maximum stable gain MSG is the appropriate power gain (Sec. 3.2). The frequency at which MAG is unity is termed f_{max} and is sometimes used to describe FET performance. However, it ignores feedback, and with $K < 1$ it becomes a meaningless figure of merit since MSG rather than MAG is the appropriate power gain. It will be seen that all of InGaAs devices fabricated--even those on graded buffer layers with no heterojunction confinement--have $K < 1$ and hence with regard to power gain would not benefit from a lower value of g_{22}. It may be, however, that the heterojunction confinement may result in a lower value of minimum noise figure NF_m.

4.1.2 Run #45 (4.3% In)

The gate lengths for these devices ranged from 1.0 to 1.1 microns and the channel doping was 0.8-1x10^{17} cm^{-3} as shown by the profile in Appendix C. Y-parameter data for two of the devices are shown in Appendix D. Table VIII summarizes the devices performance for this run.

TABLE VIII: Device Performance for Run #45

1. Y-parameter power gain:

Device #	Power Gain at 8 GHz (dB)
45- 3	19 dB(MSG)
45-11	15.5 dB(MAG)

2. Measured power gain:

Device #	f(GHz)	MAG(dB)
45- 3 (microstrip mounting)	7	14.9
"	10	10
45- 4 (ML-7 package)	7	18.7
"	10	15
45-13 (ML-7 package)	7	19
"	10	15.5

3. Minimum noise figure measurement:

Device #	f (GHz)	NF_m(dB)	G_a (dB)
45- 3	4	4.1	7.1
"	6	4.0	6.6
"	8	5.8	6.6
45-11	4	4.0	8.5
"	6	5.0	8.1
"	8	6.7	3.9

The large value of MSG = 19 dB for #45-3 is of interest. Referring to Fig. 28, expressions for g_{21}, b_{21}, g_{12}, and b_{12} were derived assuming for simplicity all parameters zero except g_m, C_1, C_2, L_s, L_g, C_{gd}, C_o, R_s, and C_4. The parameter values were then iteratively determined to give the best fit to the y-parameter data in Appendix D. MSG was then computed using Eq. (3-35) and is shown plotted along with the measured values in Fig. 37. Also shown is the computed value of MSG if L_g were zero and if both L_g and L_s were zero. It is clear that at 8 GHz these inductances are responsible for around 4.3 dB of gain through inductive peaking. For this analysis the effects of L_g on y_{12} were ignored for the sake of simplicity, so the increase in gain due to L_g and L_s might actually even be more. Basically, L_g increases y_{21} while L_s then steers y_{12} towards the optimum values given by Eqs. (3-44) and (3-45). By tweaking L_g and L_s MSG can be made to rise to 23 dB, but by this time time probably $K > 1$ so that MAG rather than MSG is the appropriate power gain to use. At any rate, Fig. 37 clearly demonstrates the role that parasitic elements can play in achieving high values of gain and demonstrates the need to be able to sort out what part of the performance is due to improved material characteristics and what part is due to the effect of parasitics.

4.2 Two-Source System

Device runs #46 to #50 were grown directly on Cr-doped GaAs substrates while runs #51 and later employed a graded lattice-matching buffer layer in an effort to obtain smooth, dislocation-free active layers. Figures 1, 2, and 3 of Progress Report No. 4 (June-July 1975) show the active layer surfaces for In concentrations of 5.3%, 10.7%, and 13.9%, respectively, clearly demonstrating the degradation in surface morphology with In concentration when no buffer layer is employed.

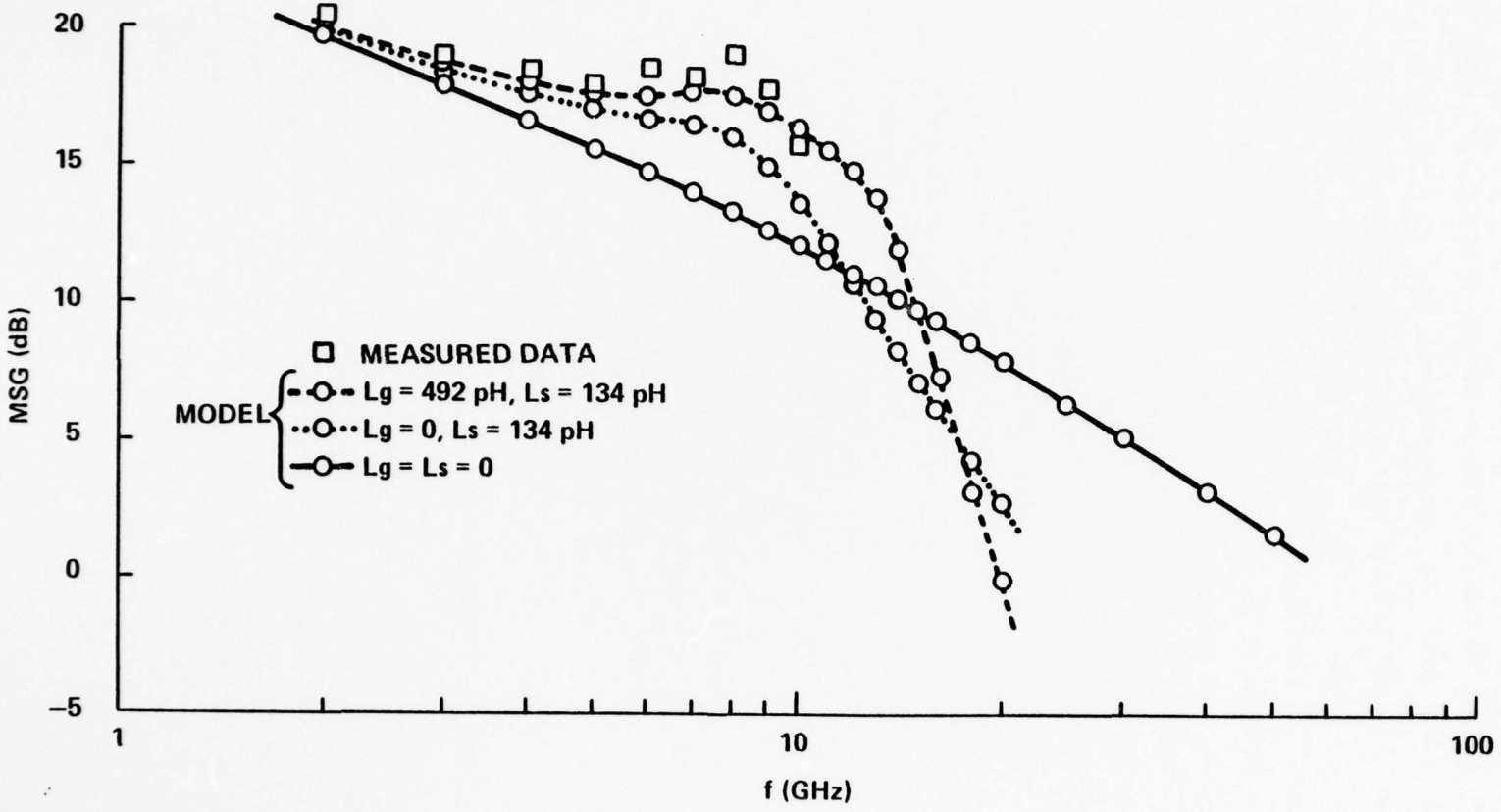


Figure 37. Gain dependence on parasitic inductances.

4.2.1 Run #46 (5.7% In)

The gate lengths for this run ranged from 0.8 to 1.1 microns and the channel doping was 1.7×10^{17} cm^{-3}. The devices exhibited quite a range of variation with I_{dss} ranging from 9 to 67 mA, V_p from 4 to 7 V, and g_m from 7 to 15 mmhos. Y-parameter data for devices #46-3, 46-8, 46-26 and 46-27 are given in Appendix D and show a wide variation in g_{ds}, from 0.69 to 2.18 mmhos at 9 GHz. These variations are greater than for previous runs and are due to lateral inhomogeneities in the active layer. Use of a two-source growth system raises the possibility of compositional variation across the wafer as well as with depth into the layer. Subsequently, a baffle was added to the reactor between the wafer and sources to enhance mixing. Table IX gives the noise figure data for this run.

TABLE IX: Run #46 Noise Figure Measurements

Device #	NF_m at 8 GHz (dB)	G_a (dB)
46-8	6.5	9.1
46-26	5.4	7.0
46-27	7.5	8.3

4.2.2 Run #48 (13.9% In)

Gate lengths ranged from 1.2 to 1.4 microns and the channel doping ranged from 3 to 5 $\times 10^{17}$ cm^{-3} as shown by the doping profile in Appendix C. The devices would not pinch-off completely, and g_m ranged from 11 to 13 mmhos. Y-parameter data for #48-21 are given in Appendix D. At 8 GHz, 8.6 dB of gain was measured in the microstrip mounting and 9.7 dB in the ML-7 package.

4.2.3 Run #50 (10.7% In)

Gate lengths ranged from 1.0 to 1.2 microns and the channel doping ranged from 1.7 to 2.5 x 10^{17} cm^{-3}. The pinch-off voltage was 6-8 V and g_m was 12-13 mmhos. Y-parameter data for several devices are given in Appendix D. The microstrip mounting gave 14 dB at 8 GHz and 11.4 dB at 10 GHz, while the ML-7 package gave 17 dB at 8 GHz.

4.2.4 Runs #51 and #52 (16% In)

Run #51 had a 2.5-micron graded buffer layer and a 0.4-micron active layer, and run #52 had a 3.4-micron graded buffer layer and a 0.34-micron active layer. The doping profiles are shown in Appendix C and reveal either incomplete compensation by the Cr and/or significant growth during the doping switch from Cr to S. The devices fabricated on these wafers would not pinch-off, had a low g_m (2-3 mmhos), and at a drain bias of around 5 V would form a shorting link between the drain and the source.

4.2.5 Run #53 (15% In)

This run had a 2.5-micron graded buffer layer with a channel doping of 10^{17} cm^{-3}. The channel doping profile is shown in Appendix C and shows a steep drop-off into the buffer layer. Figure 38 shows the drain characteristic of one of the devices.

Y-parameter measurements for several of the devices are shown in Appendix D giving gains ranging from 13 to 15 dB at 8 GHz. Table X summarizes actual measurements made on the devices.

The g_m values for #53-0 and 53-11 were measured using 0.1-V steps on the gate while the rest were done with 1-V steps, thereby giving higher and more accurate values of g_m.

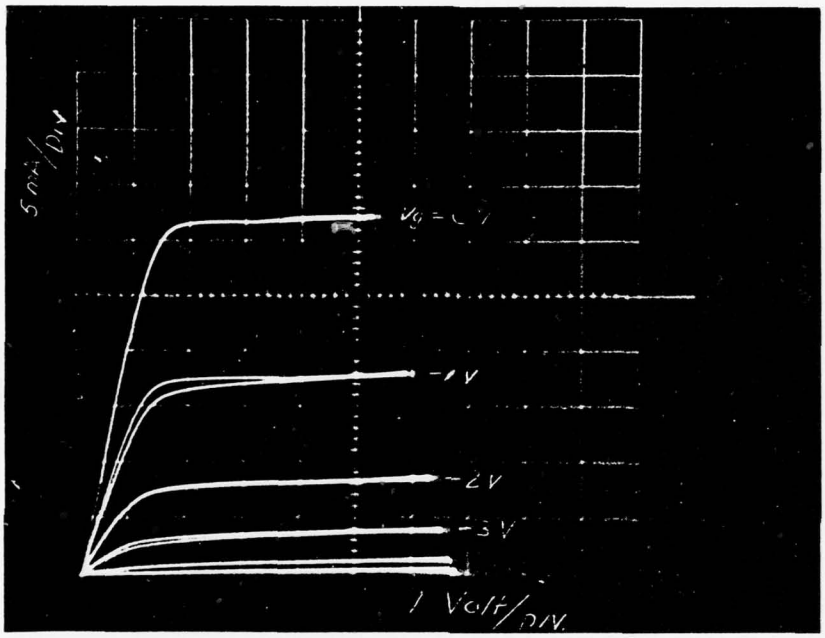


Fig. 38. 15% In FET drain characteristic.

TABLE X: Device Performance for Run #53

Device #	g_m (mmho)	L (micron)	R_s (ohm)	MAG (dB) 8 GHz	MAG (dB) 11 GHz	NF_m @ 8 GHz (dB) NF_m	NF_m @ 8 GHz (dB) G_a
53- 0	22	1.33	8	14.5	12.5	4.4	6.7
53- 1	18	-	-	14.2	12.6	-	-
53- 4	13	-	-	13.4	-	4.04	6
53- 7	18	-	-	14.1	12.4	-	-
53- 8	17.5	-	-	14.5	12.5	-	-
53- 9	-	-	-	14.3	12.5	-	-
53-10	17.5	1.36	10.3	14	12.6	4.45	7.8
53-11	23	1.42	9	14	12.4	4.4	8.4
53-12	17	1.4	-	14	12	5.3	6.7
53-13	17	1.5	-	12.6	-	7.1	5.8
53-14	17	1.3	-	13.8	-	3.5	4
53-15	17	1.3	-	13.2	-	3.89	5.7

With R_s = 9 ohms and x_{12}= 0 at 7.7 GHz, the y-parameter data for #53-11 was fit to 0, 3, and 6 dB/octave slopes and the program described in Sec. 3.3 was used to compute the model parameters shown in Fig. 28. The results are given in Table XI.

TABLE XI: Model Parameters for #53-11

R_s =	9 ohms	C_{gd} =	0.0145 pF
C_1 =	0.0737 pF	C_o =	0.0305 pF
C_2 =	0.101 pF	C_3 =	0.178 pF
r_c =	80.6 ohms	C_4 =	0.0674 pF
g_m =	26.2 mmhos	L_s =	221 pH
g_{ds} =	1.12 mmhos		

The average drain-gate spacing was around 1 micron, but does get as low as 0.7 micron in some places. Equation (34) of Ref. 37 simply gives C_{gd} as the interelectrode capacitance between parallel metal strips on top of GaAs, and mentions that this formula tends to overestimate the experimental values. Indeed it does, since the formula gives 0.025 pF while only 0.0145 was measured. This formula ignores the shielding effect of the depleted epitaxial layer under the gate (which should shield the underside of the gate from the drain) and also ignores the shielding effect of the source which for run #53 was symmetrically located on the other side of the gate from the drain. When all of this shielding is taken into account, the metallization capacitance is reduced by an approximate factor of 26 to around 0.001 pF, which is much less than the measured value. The discrepancy can be attributed to the Schottky-barrier edge capacitance on the drain side of the gate. Evaluation of this capacitance using a crude analysis gave a value of 0.011 pF which when added to the 0.001 pF of the metallization capacitance gives a value close to the 0.0145 pF actually measured. One theory has it that the low value of C_{gd} is due to a stationary Gunn domain on the drain edge of the gate which can extend out towards the source a distance of almost a micron.[43] At any rate, it would appear that C_{gd} cannot be appreciably diminished by increasing the drain-gate spacing or decreasing the gate length as suggested by Eq. (34) of Ref. 37. From the y-parameters for #53-11 at 8 GHz, the optimum value of b_{12} is 0.264×10^{-3} mmhos by Eq. (3-45). To achieve this, C_{gd} would have to be reduced to 0.00684 pF if L_s were to remain the same. Since

$$b_{12} \cong -\omega C_{gd} + \frac{\omega^3 L_s (C_{gs}+C_3)(C_o+C_4)}{1-\omega^2 L_s (C_{gs}+C_3+C_o+C_4)} \qquad (4\text{-}1)$$

the same result could be obtained by increasing L_s to 267 pH. Of course the effect on g_{12} would also have to be considered.

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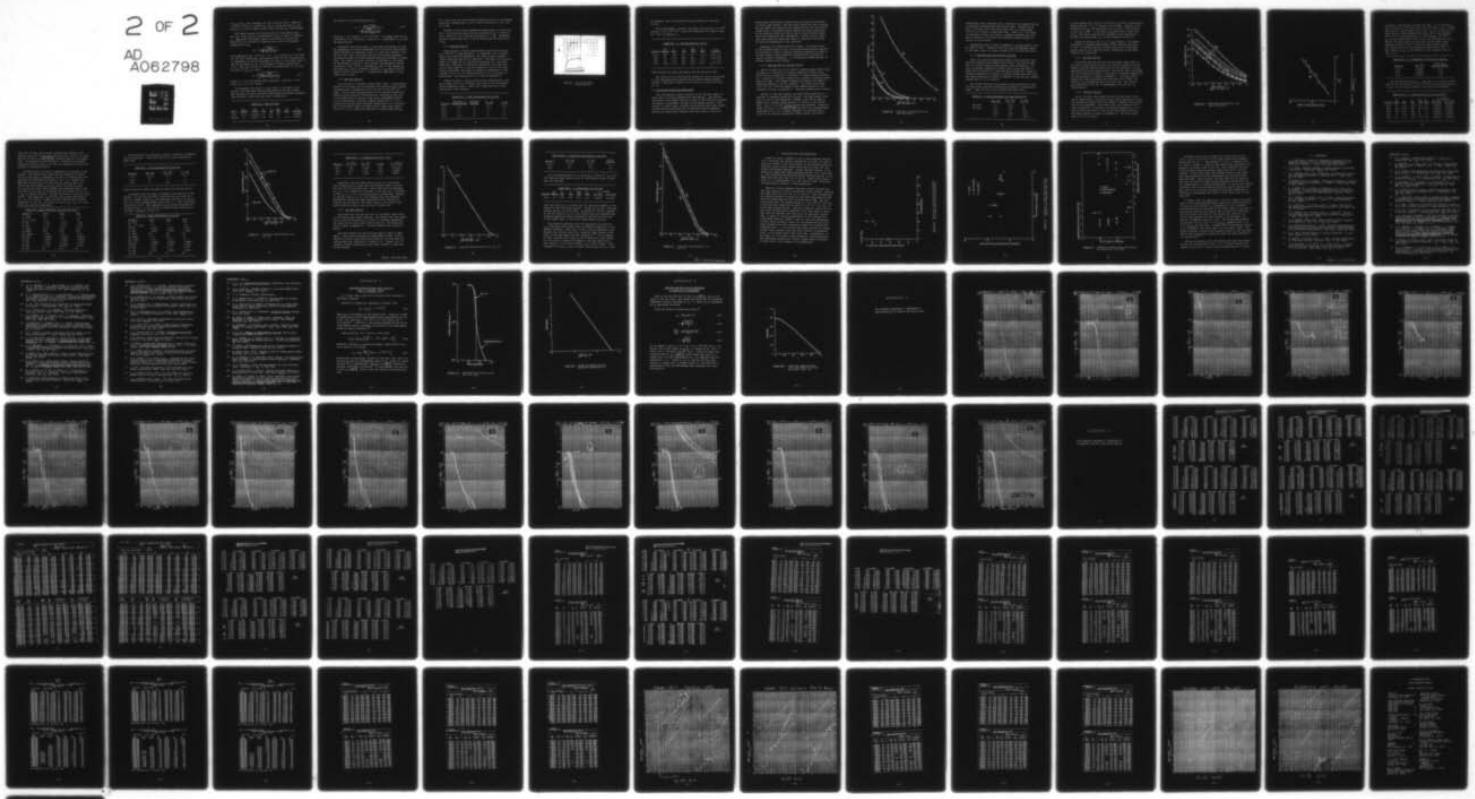

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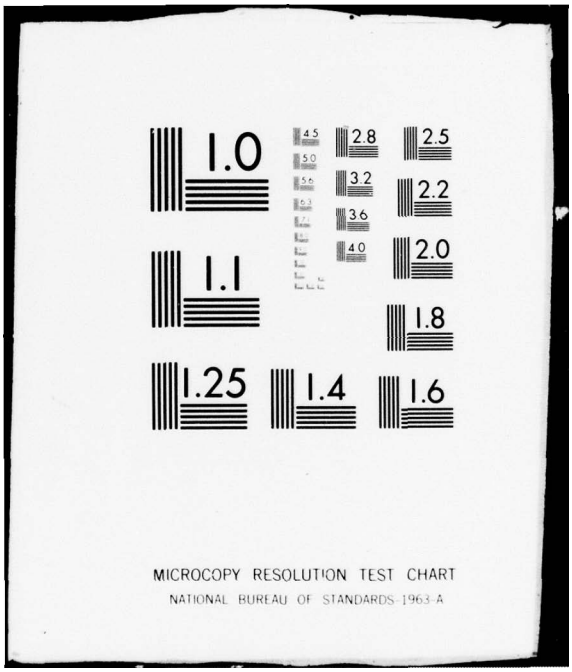
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If g_{12} and b_{12} were optimum, the gain would be 19 dB. Reducing L would do little to increase g_m, but it would decrease C_{gs} and hence g_{11} to give a higher value of MSG provided y_{12} were optimum.

The channel length for these devices is sufficiently long that Eq. (3-30) may be in considerable error if used to estimate v_s. Retaining first-order terms in the theory of Turner and Wilson[40] as L is allowed to approach zero gives the following expression for g_m

$$g_m = Zv_s\sqrt{\frac{\epsilon q N_D}{2(\phi_B - V_g + E_s L)}} \quad , \tag{4-2}$$

which reduces to Eq. (3-16) as $L \to 0$. E_s is around 3.5×10^3 V/cm for 10^{17} cm^{-3} doped GaAs, and assuming that the low field mobility is independent of the In percentage at least to first-order (Fig. 8) then by the model of Fig. 1 E_s should be linearly proportional to v_s. With ϕ_B= 0.68 eV for 15% In[61] and accounting for the self-bias due to I_{dss} R_s, using

$$v_s = \frac{g_m}{Z}\Bigg/\sqrt{\frac{\epsilon q N_D}{2(\phi_B + I_{dss}R_s + E_s L}} \tag{4-3}$$

gives $v_s = 2.2 \times 10^7$ cm/sec using iteration. Using Eq. (3-18) gives $v_s = 2.13 \times 10^7$ cm/sec.

To determine the value of v_s for GaAs for the sake of comparison, two GaAs FETs (#SAL-90 fabricated by the Solid State West Division of Varian and #35-A fabricated by Corporate Research) were measured, giving the data shown in Table XII.

TABLE XII: GaAs FET Data

FET #	g_m (mmhos)	N_D (cm^{-3})	L (μm)	Z (μm)	I_{dss} (mA)	R_s (ohm)	v_s (cm/sec)
35-A	18.75	1.2×10^{17}	1.5	207	41	7	1.31×10^7
SAL-90	15	1.1×10^{17}	1.12	192	36	11.3	1.23×10^7

The values of v_s were determined from

$$v_s = \frac{g_m/(1-R_s g_m)}{Z\sqrt{\frac{\epsilon q N_D}{2(\phi_B + I_{dss} R_s + E_s L}}} \qquad (4\text{-}4)$$

using ϕ_B = 0.8 V and E_s = 3.5 x 10^3 V/cm. It appears that the 15% In devices of run #53 enjoy a factor of 1.7 improvement in v_s over the GaAs devices.

Concerning the noise figure, it was with this device run that the phenomenon of velocity degradation at the active layer-buffer layer interface as discussed in Sec. 3.4 was first noticed. This did not occur until after runs #54 and 55 had been completed, and hence no effort was made towards solving the problem for these runs. The intent for these runs was to determine v_s for higher In percentages, decrease L, and increase the gate-drain spacing. Decreasing L does little to increase g_m, but it does reduce C_{gs} and hence g_{11}, and an attendant reduction in C_{gd} should lead to higher values of power gain. A significant improvement in NF_m should also be seen.

4.2.6 Run #54 (18% In)

This run had a 7.4-micron graded buffer layer. A good doping profile of the wafer was not obtained, but from pinch-off voltage considerations it appeared to be in the low to mid 10^{16} cm^{-3} range. The dc drain characteristics of the devices showed good saturation and pinch-off characteristics, although g_m was only 7 to 15 mmhos with R_s having a high value, presumably because of the lower doping. The gate lengths ranged from 1.1 to 1.3 microns and the gate-drain spacings ranged from 2 to 2.5 microns. All of the devices would oscillate above a drain bias ranging from 2.8 to 3.4 V, making it difficult to measure MAG and NF_m.

At a drain bias just below where oscillation sets in, the maximum power gain ranged from 6.4 to 11.5 dB at 8 GHz and 4.7 to 9 dB at 10 GHz.

Appendix D gives the y-parameters measurements for #54-5 and 54-6. The noise was high with NF_m occurring at $V_g = 0$ and having a value of 12 to 14 dB with G_a being 4 to 5 dB. Supposedly the poor results were due to the low doping and the high value of R_s.

4.2.7 Run #55 (34% In)

This run had a 2-micron graded buffer layer and was grown on a 10^{18} cm^{-3} n-type substrate. As expected, the rf performance of the FETs was degraded by the large parasitic capacitances resulting from the n^+ substrate. The wafer was initially grown as a dummy run for calibration purposes at a time when there was a shortage of insulating substrates, but since the active layer grown on it was far superior to any of the other high In percentage runs made on insulating substrates, it was decided to use it to at least determine v_s for the higher In percentages. The doping profile is shown in Appendix C.

Figure 39 shows a typical device drain characteristic. The g_m's ranged from 26 to 29 mmhos, which are by far the highest values observed to date. Table XIII summarizes the rf data obtained for these devices.

TABLE XIII: 8 GHz Performance for Run #55

Device #	MSG From y-Parameters (dB)	Measured Gain (dB)	NF_m (dB)	G_a (dB)
55-3	10.7	--	14.3	4.8
55-5	---	11	---	---
55-6	11	11	12	5.3
55-7	11.1	13	---	---

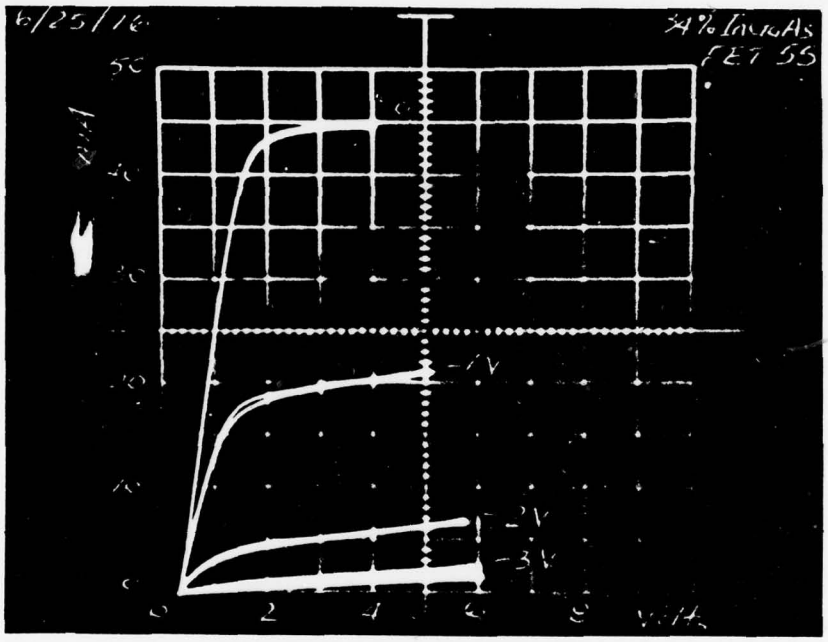

Fig. 39. 34% In FET drain characteristic.

As expected, the rf performance was poor because of the parasitics.

The dc performance, however, was good, and using ϕ_B = 0.4 eV[61] and $N_D = 1.25 \times 10^{17}$ cm^{-3}, Table XIV summarizes the results using Eq. (4-4) to compute v_s.

TABLE XIV: v_s Calculations for 34% In

Device #	g_m (mmhos)	L (μm)	Z (μm)	I_{dss} (mA)	R_s (ohm)	v_s (cm/sec)
55-3	29	1.36	217	48	5.3	1.94×10^7
55-5	29	1.35	218	26.5	9.3	2.18×10^7
55-6	26	1.18	220	25.5	11.4	2×10^7
55-7	26.8	1.47	216	20.5	10.5	2.15×10^7

These results are about the same as for the 15% In run #53.

The effect of the lower barrier height for 34% In can be seen in the increased gate-to-source and/or -drain reverse leakage current. Typically it was 0.1 to 0.2 μA at 1 V and 10 to 25 μA at 3 V.

4.3 Two-Source System With Heat Pipes

With the previous reactor system, out of the many wafers gr grown only a few were processed for FET devices. This was because most of the wafers had one or more of the following problems: low doping, too gradual a falloff in the doping profile, a non-insulating buffer layer, hillocks which prevent good mask contact, and bad surface morphology due to excessive lattice-mismatch. Besides the temperature gradient along the source, there was a

doping delay and possibly growth during the switch from buffer to active layer growth. The heat pipes solved the first problem, but the latter two problems still persisted with the new reactor system until a new dopant mixing chamber and better regulation of the relative flows over the Ga and In sources during slight vapor etch conditions were implemented. Device quality wafers were then grown and steps were taken to alleviate the problem of velocity degradation at the interface.

Beginning with wafers from this reactor, all devices were of the geometry shown in Fig. 36 and used electron-beam exposure of the gates in order to achieve controlled exposure of rough or hillocky wafers, which cannot be satisfactorily processed by optical contact lithography. It incidentally became possible to achieve submicron gate lengths.

4.3.1 Runs #56 (8% In) and #57 (9% In)

The 8% In wafer had a 10.7-micron linearly-graded buffer layer followed by 3.6 microns of constant composition buffer layer, while the 9% In wafer had 6.3 microns of linear grading followed by 1.6 microns of constant composition, assuming a constant growth rate with time. The constant composition layers were added to hopefully improve v_s at the interface. The layers were doped 3-4 x 10^{17} cm^{-3} with the desired rapid doping falloff at the interface as shown in Appendix C. The gate lengths were 1 micron.

Because of the high doping, the layers were grown thin to maintain a reasonable pinch-off voltage. The gate sputter etch prior to the Pt gate deposition (needed to get the Pt gate to adhere well) removed enough material to result in low current FETs. Only 5 to 20 mA of drain current was obtained. Figure 40 shows the plot of I_d vs $\sqrt{\phi_B - V_g + I_d R_s}$ and using the interpretation developed in Sec. 3.4 it seems reasonable to conclude that in spite of the constant composition buffer layers, the active

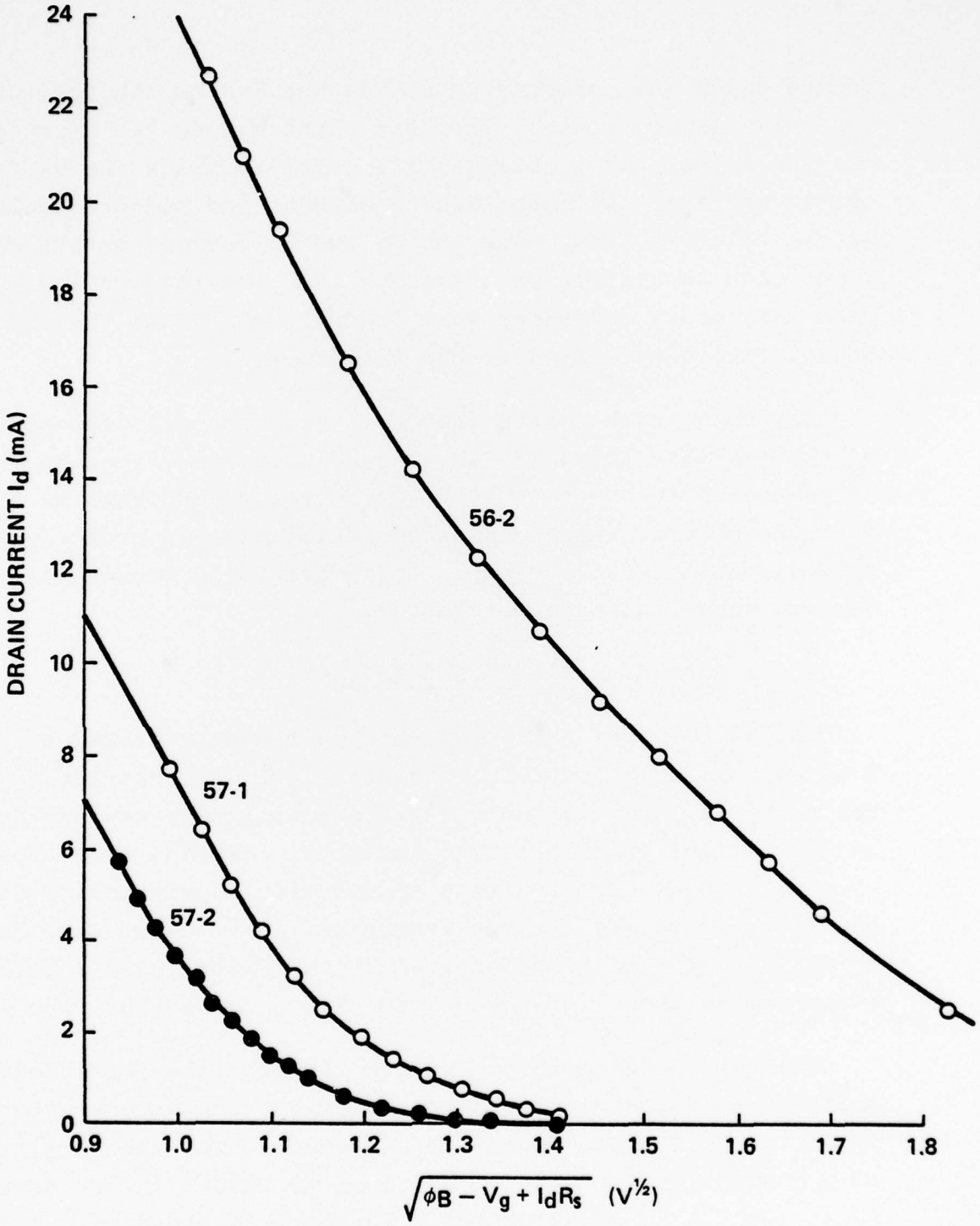

Figure 40. Pinch-off characteristic for runs #56 and 57.

layer-buffer layer interface still influences the channel quality a significant distance into the active layer. Application of Eqs. (3-19) and (4-4) both give values for v_s of only around 0.8-1.0 x 10^7 cm/sec at zero gate bias. Since 1.3 x 10^7 cm/sec is obtained for GaAs, and since v_s steadily degrades from zero bias to pinch-off, evidently the interface effects extend all the way to the surface.

Y-parameter data is shown in Appendix D, giving around 13 dB for MAG at 8 GHz. Because of the thin velocity-degraded layers R_s was high, being 11.5 ohms for #56-2 and 17.3 ohms for #57-2.

4.3.2 Runs #58 (10% In) and #59 (8.5% In)

Again the constant composition buffer layer was used, this time with thicker lower-doped active layers. The 10% In wafer had a 7- micron linearly-graded buffer layer followed by 1 micron of constant composition buffer layer, while the 8.5% In wafer had 5.8 microns of linear grading followed by 1 micron of constant composition, assuming a constant growth rate with time. The doping profiles are shown in Appendix C, and the gate lengths ranged from 0.7 to 0.8 micron.

The devices from both runs tended to Gunn oscillate at near zero gate bias, possibly preventing attainment of higher power gains. Table XV the rf data obtained for these runs.

TABLE XV: 8 GHz Performance for Runs #58 and 59

	MAG (dB)	NF_m (dB)	G_a (dB)
Run #58:	---	2.54	11
Run #59:	16.2	1.86	10
	16.9	2.7	11.8
	18.9	2.05	12.1
	---	2.3	12.9

It thus appears that even at 8.5-10% In v_s is still significantly higher than the 1.3×10^7 cm/sec value of GaAs. Because of the high value of C_{gs}, the computation of v_s by Eq. (3-18) results in very low values. A low value of ϕ_B would give a high value of C_{gs}, but then g_m should also increase by the same factor. But per unit gate width, g_m, is about same as for #53-11.

Figure 42 gives a plot of R_s vs L_{sg}/d where d, the channel thickness, is assumed proportional to the abscissa intercept in Fig. 41, showing that R_s is mainly due to the source-gate spacing and not the specific contact resistance of the metallization for these runs.

4.3.3 Run #60 (14% In)

This wafer had the last part of the buffer layer grown in the active layer growth position to avoid any effects that the change in growth position might have on the interface in going from buffer to active layer growth. The buffer layer was graded for 12.6 microns followed by 1.1 microns of constant composition. The doping profile is shown in Appendix C. For some unknown reason the source resistance was very high (40-50 ohms), resulting in g_m compression near zero gate bias. The devices were useless not only for rf measurements but also for v_s determination.

4.3.4 Run #61 (16% In)

As for run #60, this wafer also had the last part of the buffer layer grown in the active layer growth position to avoid any deleterious effects that the change in growth position might have on the interface. The buffer layer was graded for 9 microns followed by 1.4 microns of constant composition, 0.3 micron of which was grown in the active layer growth position. The doping profile is shown in Appendix C. The gate lengths were 0.7 to 0.75 micron.

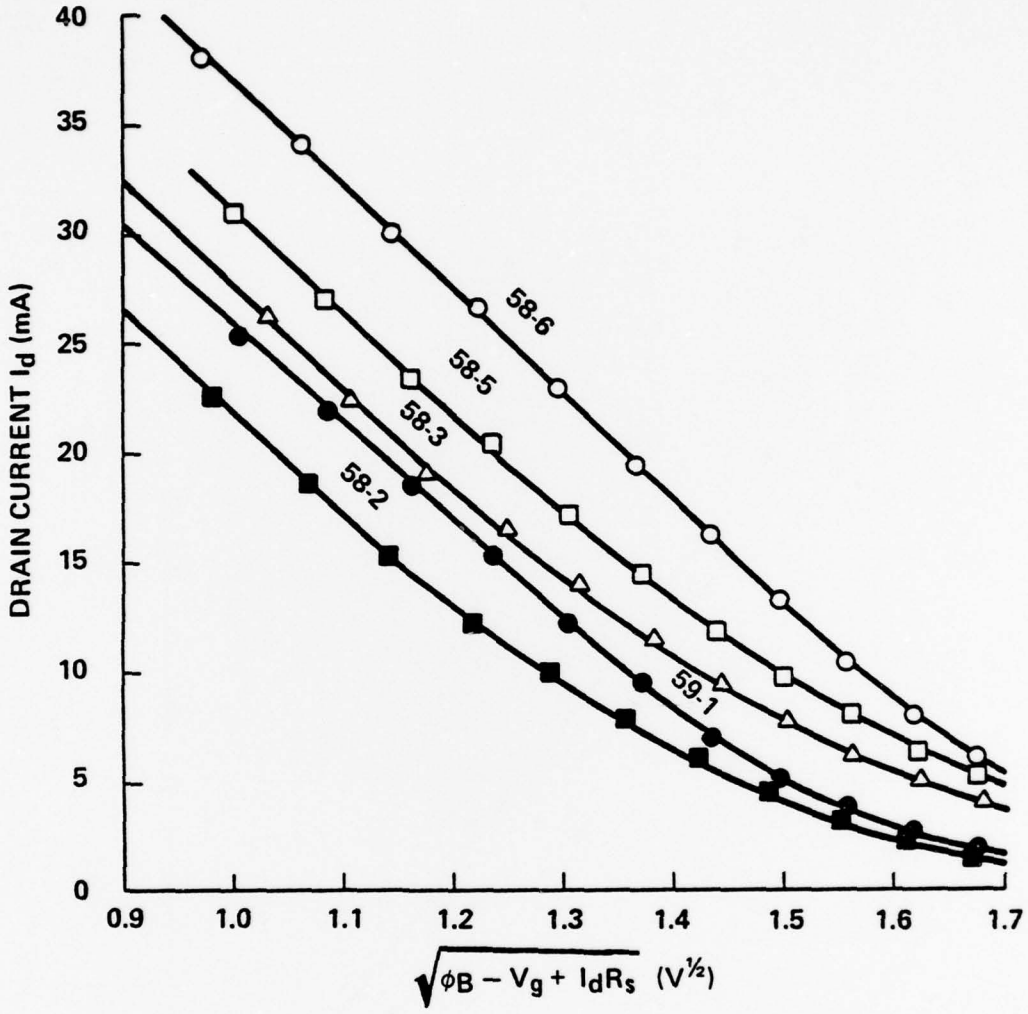

Figure 41. Pinch-off characteristic for runs #58 and 59.

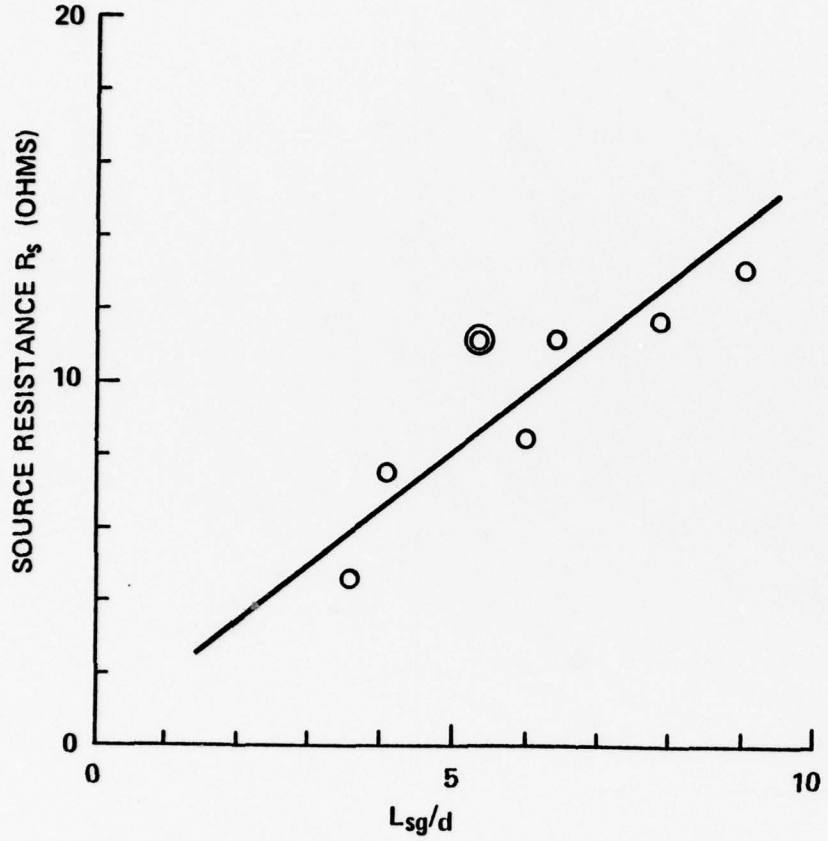

Figure 42. Correlation of R_s with source-gate spacing L_{sg}.

In general, the devices are about the same. It is surprising that, in spite of the lower value of R_s for #58-6, g_{12} is higher, resulting in a much higher value of C_o. C_{gs} is 0.25 pF for all three devices, which exceeds by a factor of two the computed value of 0.12 pF assuming ϕ_B= 0.77 eV[61] and $N_D = 10^{17}$ cm^{-3}. C_{gs} is even higher than the 0.174 pF value obtained for #53-11, and yet the gate length is about half and the width three-quarters of that for #53-11, with the same channel doping. Also, Table XVII that the gate-drain spacing has little, if any, effect on C_{gd}, giving support to the arguments given in Sec. 4.2.5.

TABLE XVII: C_{gd} Dependence on Gate-Drain Spacing

Device #	C_{gd} (pF)	Gate-Drain Spacing (micron)
58-3	0.00845	0.97
58-6	0.00692	1.84
59-1	0.00752	2.66

For the determination of v_s, using ϕ_B = 0.77 eV for run #58 and 0.79 eV for run #59,[61] $N_D = 10^{17}$ cm^{-3} and the slopes given in in Fig. 41, the results shown in Table XVIII are obtained.

TABLE XVIII: v_s Calculations for 8.5% and 10% In

Device#	g_m (mmho)	L (μm)	Z (μm)	I_{dss} (mA)	R_s (ohm)	v_s (cm/sec) Eq.(4-4)	v_s (cm/sec) Eq.(3-19)
58-2	19	0.83	147.5	22.5	8.5	1.98×10^7	1.74×10^7
58-3	18.6	0.78	148	26.2	11.2	2.21×10^7	1.74×10^7
58-5	20	0.71	148	31	7.5	2.29×10^7	1.74×10^7
58-6	21	0.74	148.5	38	4.6	1.94×10^7	1.74×10^7
59-1	18	0.74	147	25.5	8.6	1.85×10^7	1.66×10^7

These are the best noise results obtained for InGaAs so far. However, NF_m still occurs near zero gate bias, and Fig. 41 shows the tail in the I_d vs $\sqrt{\phi_B - V_g + I_d R_s}$ typically seen for the InGaAs FETs. As deduced for runs #56 and 57, evidently the constant composition buffer layer is not able to completely alleviate the problem of interface effects.

Y-parameter data are shown in Appendix D for several of the devices. The devices were tested both at WATS and at Varian, and the plots shown in Appendix D for #58-3 illustrate well the problems and differences discussed in Sec. 3.3. Whereas the WATS data give good g_{11} data but poor g_{21} and b_{21} data, the Varian data gives good g_{21} and b_{21} data, but poor g_{11} data. The g_{22} data for #58-5 rises steeply with frequency from a very low value which cannot be accounted for by the model of Fig. 28 if g_{ds} is assumed constant. Perhaps the device is close to oscillation. Upon measuring R_s and using the program described in Sec. 3.3, the results in Table XVI were obtained for the model parameters of Fig. 28. The data for each of g_{11}, b_{11}, etc. were taken from the best measurement.

TABLE XVI: Model Parameters for Runs #58 and 59

Device #	58-3	58-6	59-1
R_s (ohm)	11.2	4.6	8.6
$f_{x12} = 0$ (GHz)	8.5	7.1	8.7
C_1 (pF)	0.103	0.105	0.106
C_2 (pF)	0.141	0.144	0.145
r_c (ohm)	14.2	19.6	13.5
g_m (mmho)	20.0	20.9	21.8
g_{ds} (mmho)	0.963	1.30	2.48
C_{gd} (pF)	0.00845	0.00692	0.00752
C_o (pF)	0.0267	0.0846	0.00217
C_3 (pF)	0.0467	0.0322	0.0196
C_4 (pF)	0.114	00.0798	0.129
L_s (pH)	132	82.9	115

These devices also oscillated, making it difficult to measure the rf performance. Table XIX gives the rf data obtained for these runs.

TABLE XIX: 8 GHz Performance for Run #61

Device #	MAG (dB)	NF_m (dB)	G_a (dB)
61-4	17.8	---	---
61-5	16	---	---
61-6	---	2.4	13

These results are about the same as those for runs #58 and 59.

Y-parameter data are shown in Appendix D for several of the devices. As was seen for #58-5, the plots for #61-1 and 61-2 reveal a steeply rising g_{22} with frequency from very low values. The rest of the parameter data seem to fit 0, 3, and 6 dB/octave lines pretty well. Upon measuring R_s and using the program described in Sec. 3.3, the results in Table XX were obtained for the model parameters of Fig. 28.

TABLE XX: Model Parameters for Run #61

Device #	61-1	61-2	61-3
R_s (ohm)	7.7	7.7	8.3
$f_{x_{12}} = 0$ (GHz)	7.6	7	7.9
C_1 (pF)	0.0405	0.0525	0.0301
C_2 (pF)	0.0554	0.0717	0.0411
r_c (ohm)	110	61.5	130
g_m (mmho)	19.1	22.3	18
g_{ds} (mmho)	1.16	0.117	1.7
C_{gd} (pF)	0.00809	0.00691	0.00948
C_o (pF)	0.0657	0.0802	0.0385
C_3 (pF)	0.121	0.12	0.157
C_4 (pF)	0.106	0.0686	0.0932
L_s (pF)	118	121	146

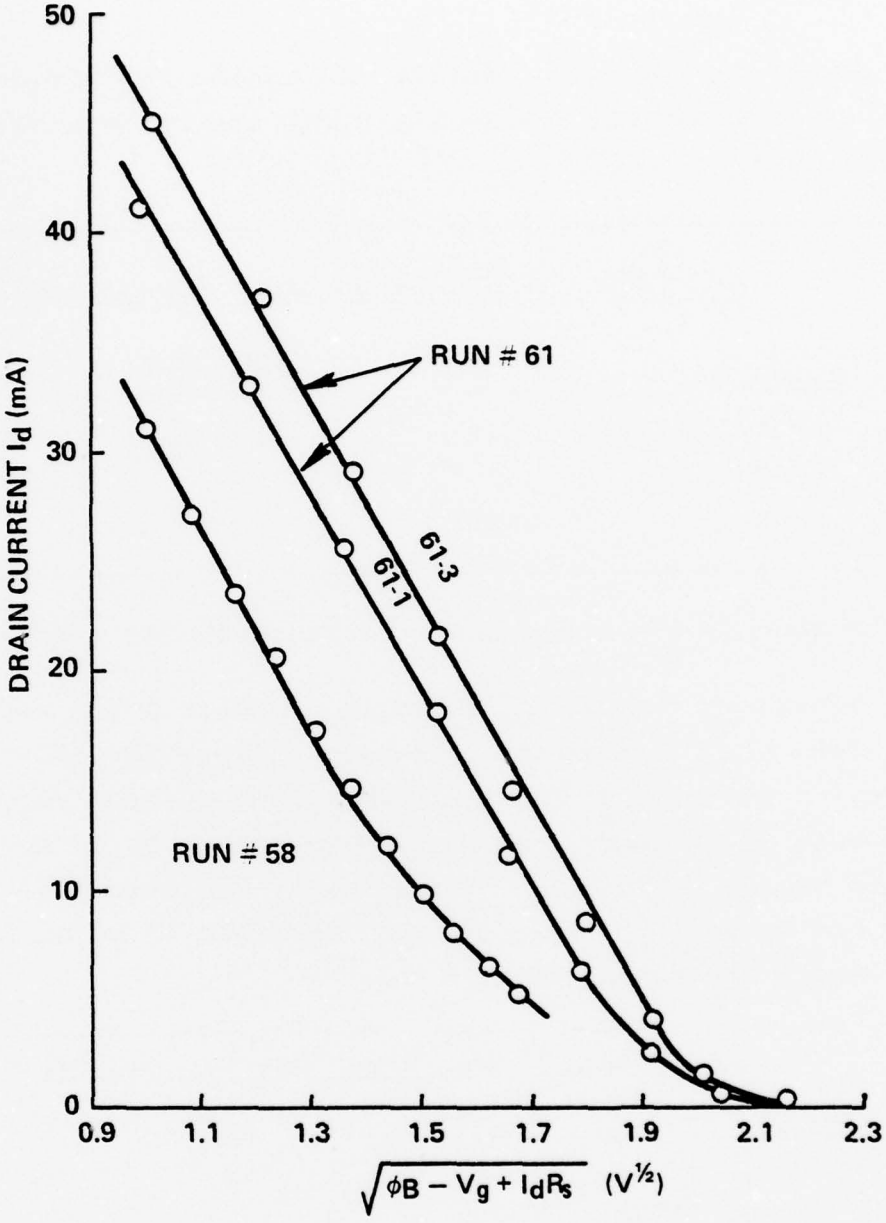

Figure 43. Pinch-off characteristic for run #61.

TABLE XXII: v_s Computation by Eq. (3-18)

Device #	g_m (mmho)	C_{gs} (pF)	L (μm)	v_s (cm/sec)
61-1	19.1	0.0959	0.81	1.61×10^7
61-2	22.3	0.124	0.69	1.24×10^7
61-3	18	0.0712	0.75	1.9×10^7

Consistent with the linear plot in Fig. 43, the minimum noise figure value in Table XIX occurred much closer to pinch-off than for the previous runs. The 2.4-dB value was measured at V_g = -1.9 V (pinch-off is around -3 V by Fig. 43) in contrast to the V_g = 0 to -0.5 V values previously encountered. Because of the low value of v_s it is not certain that the interface degradation problem has been alleviated by the technique of growing the last part of the buffer layer in the active layer growth position since v_s was not high to begin with.

4.3.5 Run #62 (15% In)

This wafer also had the last part of the buffer layer grown in the active layer growth position. The buffer layer was graded for 7.6 microns followed by 0.8 micron of constant composition all grown in the active layer growth position. The doping profile is shown in Appendix C. The gate lengths were around 0.5 micron.

The noise figures for this run were high as shown in Table XXIII. Oscillation prevented the measurement of MAG. As was found for run #61, NF_m occurs much closer to pinch-off than for the previous runs (pinch-off is around -3 V). Indeed, Fig. 44 reveals a linear characteristic and hence constant v_s over most of the channel.

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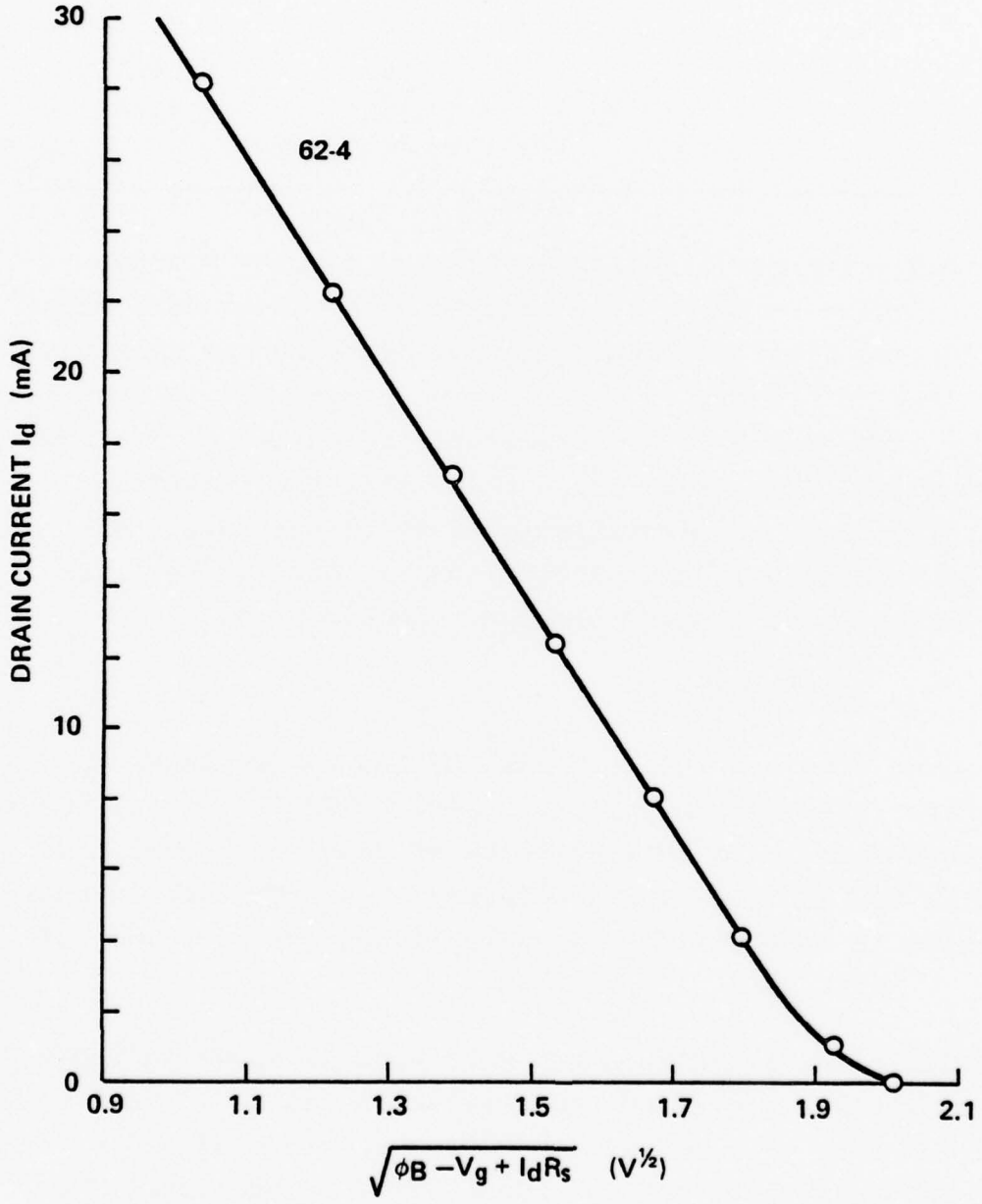

Figure 44. Pinch-off characteristic for run 62.

TABLE XXIII: 8 GHz Noise Performance of Run #62

Device #	NF_m (dB)	G_a (dB)	Gate Bias (V)
62-5	4.75	11.8	-1.7
62-6	5.7	8.6	-2.1

For the determination of v_s, using ϕ_B = 0.68 eV,[61] $N_D = 10^{17}$ cm^{-3} and the slope given in Fig. 44, the results shown in Table XXIV are obtained.

TABLE XXIV: v_s Computation for Run #62

Device#	g_m (mmho)	L (μm)	Z (μm)	I_{dss} (mA)	R_s (ohm)	v_s (cm/sec) Eq.(4-4)	Eq.(3-19)
62-4	12	0.54	153	28.2	13.8	1.14×10^7	1.11×10^7

This low value for v_s is below that for GaAs and probably is the reason for the high noise figures. Unlike for run #61, the wafer surface quality was quite good. As stated for run #61, because of the low value of v_s it is not certain that the interface degradation problem has been alleviated by growing the last part of the buffer layer in the active layer growth position.

One possible explanation for the apparently low value for v_s is the short gate length which is becoming comparable to the channel thickness. When this is true, the gate depletion layer becomes more circular than flat, requiring more voltage to deplete to the same depth and thus reducing g_m.[65] As an example of this, although #59-1 had a g_m of 18 mmhos and a gate length of 0.74 micron, a device fabricated on the same wafer with a gate length of 0.15 micron yielded a g_m of only 6 mmhos. Thus, although the actual v_s may be higher, the analysis gives a lower

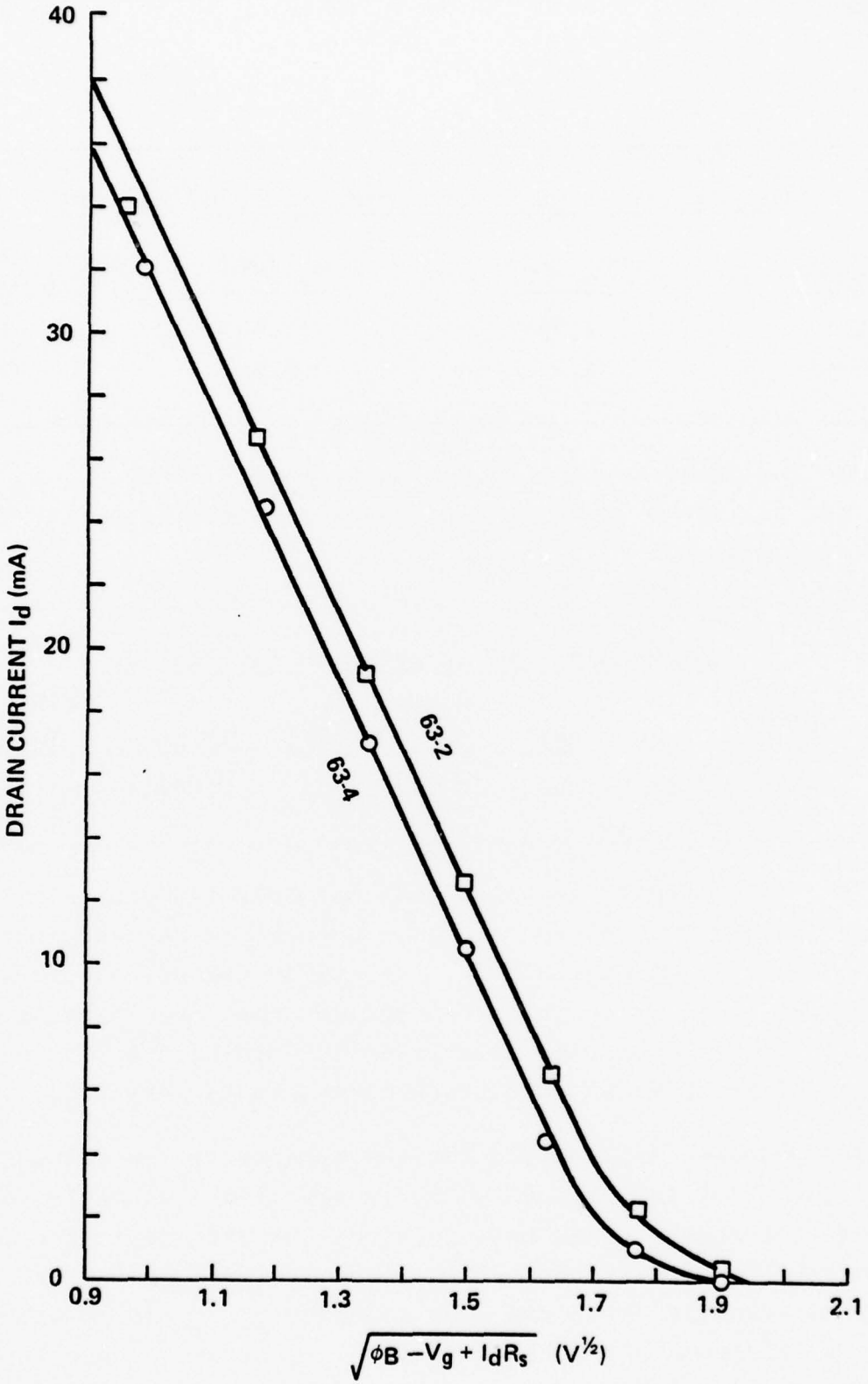

Figure 45. Pinch-off characteristic for run #63.

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5. CONCLUSIONS AND RECOMMENDATIONS

Figure 46 shows a summary of the v_s data obtained using Eq. (4-4), excluding the results obtained for runs #61, 62, and 63 which are thought to be lower because of bad surfaces and/or g_m reduction owing to gate lengths which were too short for the channel thicknesses employed. Values obtained from Eq. (3-19) essentially agree with those obtained from Eq. (4-4), while bad C_{gs} data prevented good data from being obtained from Eq. (3-18). These data show that from 10% to 34% In, InGaAs enjoys about a factor of 1.5 improvement in v_s over that for GaAs, confirming the expectations outlined in the Introduction.

Figures 47 and 48 summarize the best results obtained for MAG, NF_m, and G_a at 8 GHz as a function of gate length. The data are taken from runs #53, 58, 59, 61, and 63. Also included are the results measured at Varian for GaAs FETs fabricated by both the Solid State West Division of Varian and by NEC. For the Varian GaAs FETs, the channel doping is 1.5×10^{17} cm^{-3} for the 1.0-micron gate length devices and 2.5×10^{17} cm^{-3} for the 0.5-micron gate length devices. Generally speaking, these plots reveal that the performance obtained so far from InGaAs is about what would be obtained from GaAs using the same gate lengths. Thus, in spite of velocity degradation at the interface and lower-doped channels, InGaAs is able to match the performance of GaAs, which provides a basis for the expectation that once these problems have been eliminated InGaAs will significantly outperform GaAs. It is believed that these results for InGaAs surpass those reported using any other ternary or quaternary alloy, or any binary alloy other than GaAs. Consequently, if any effort is to be made on other materials towards extending FET performance beyond that of GaAs, InGaAs should certainly be among them if not foremost for consideration.

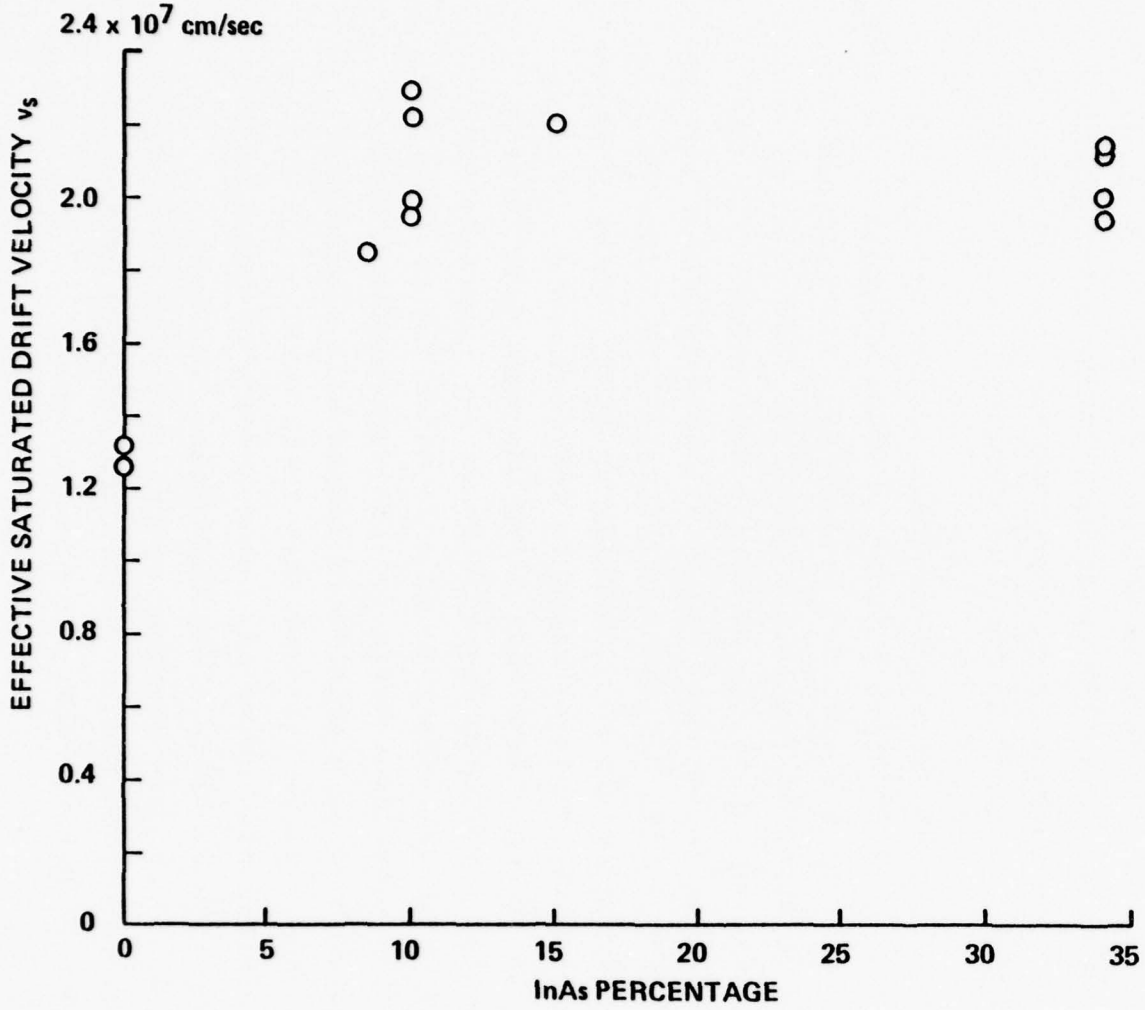

Figure 46. Effective saturated drift velocity as a function of InAs percentage.

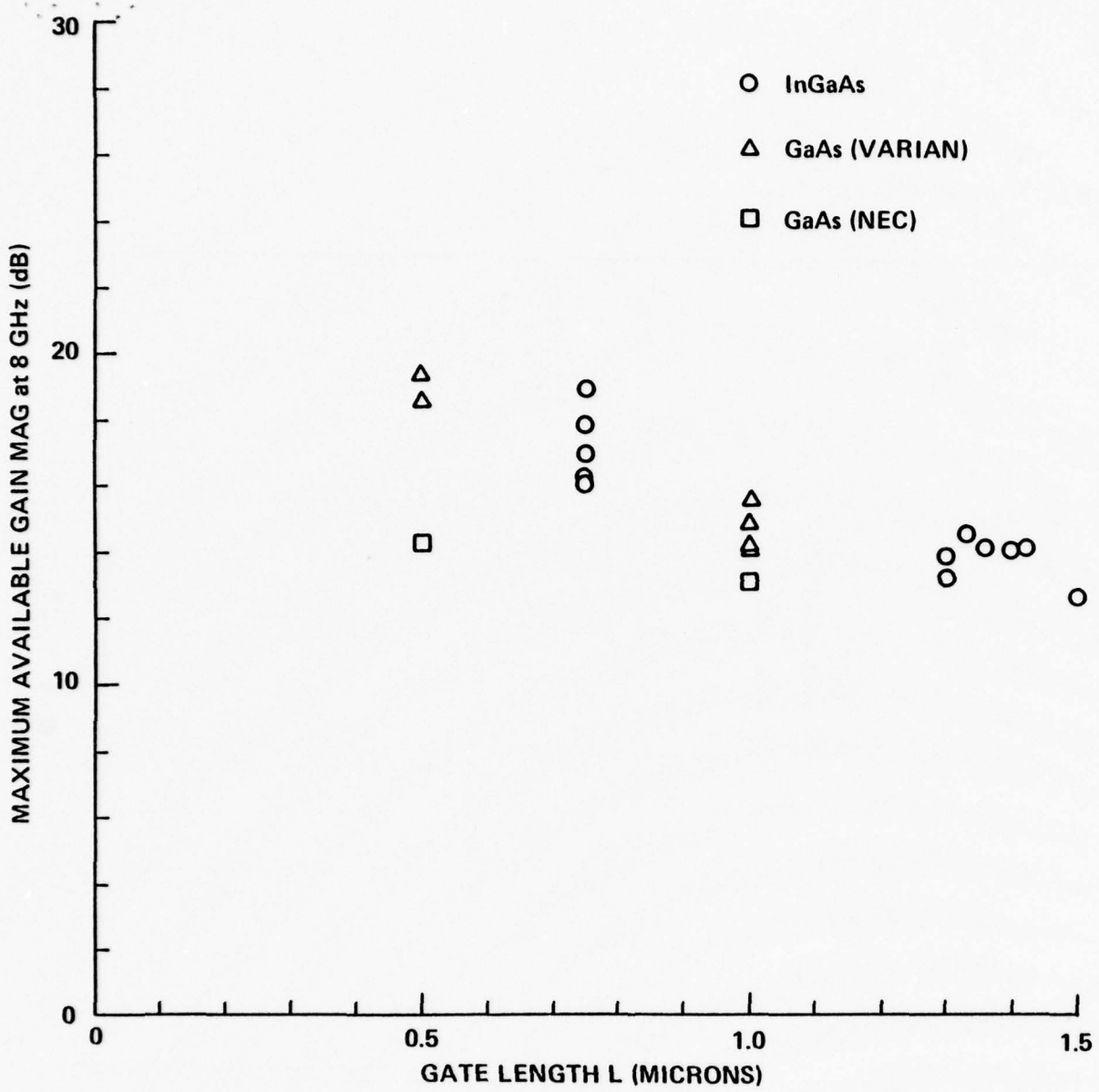

Figure 47. Summary of InGaAs power gain performance and comparison with GaAs.

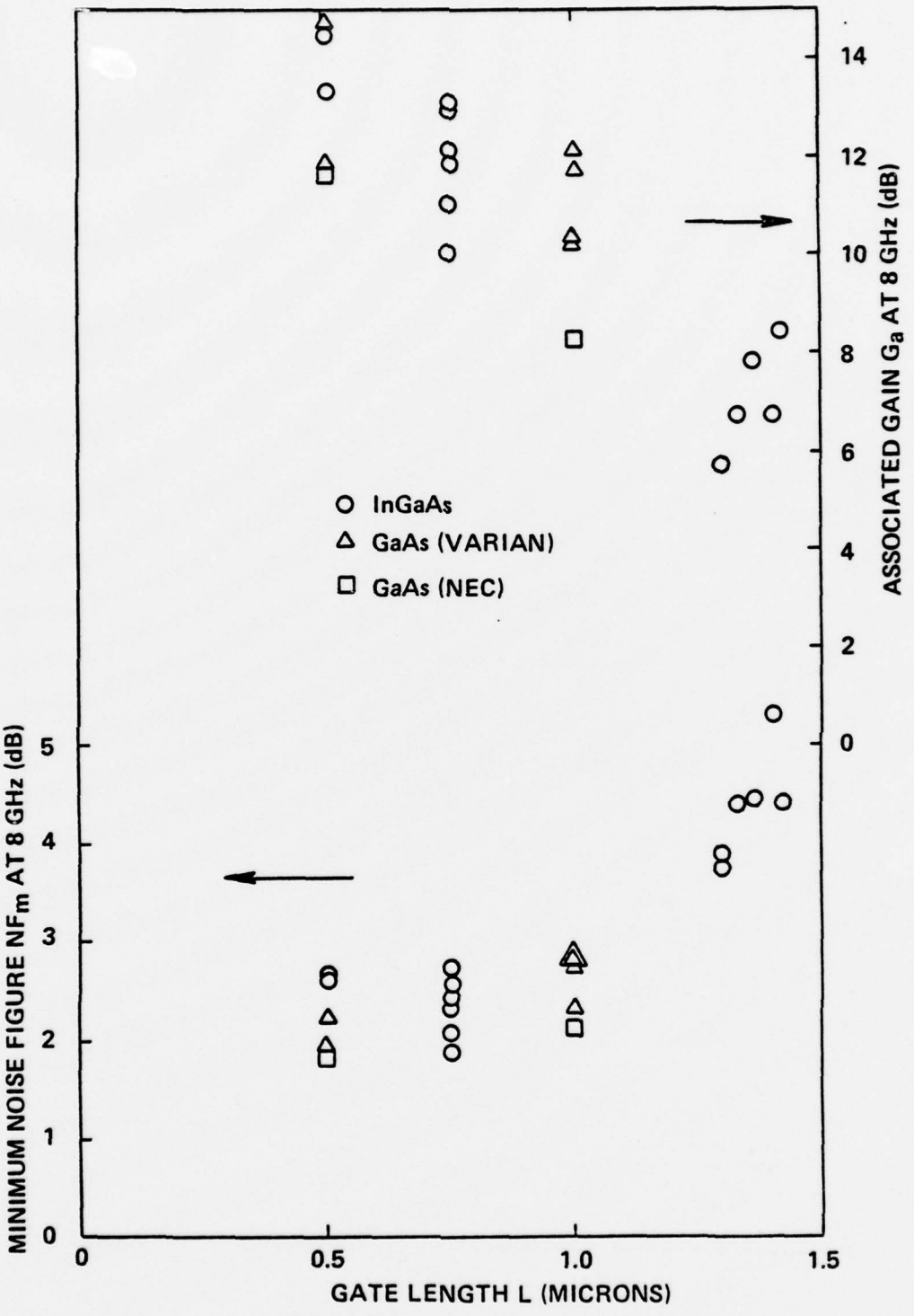

Figure 43. Summary of InGaAs noise performance and comparison with GaAs.

A program was written to compute the values given by Eqs. (3-32), (3-33), and (3-34) for the lossy terminations needed to achieve MSG for $K < 1$. When applied to #61-2, a computed value of 2 ohms is needed at 8 GHz for the input series resistance termination to achieve a MSG of 20.6 dB. This contrasts with the 16-18 dB values actually measured (Table XIX) for a 3 dB difference. On the other hand, the measured values of gain agree with those computed from the y-parameters for the Solid State West GaAs FETs. When analyzed, the GaAs FETs did not appear to need the low values of input series resistance termination that the InGaAs FETs do to achieve maximum gain. It may be that alumina substrates used in the microstrip amplifier used to measure MAG, NF_m, and G_a are too lossy to achieve the optimum terminations, resulting in performance loss which is more severe than for the GaAs FETs.

It appears that the addition of a constant composition buffer layer to the linearly-graded buffer layer did little if anything to alleviate the problem of v_s degradation at the interface. Although growing the last part of the buffer layer in the active layer growth position did improve the v_s profile and cause NF_m to occur nearer to pinch-off, the device runs (runs #61, 62, and 63) were plagued with lower values of v_s throughout the channel to somewhat cloud the issue. The closest NF_m occurred to pinch-off was at 0.25 to 0.35 I_d/I_{dss}, compared with 0.1 to 0.15 I_d/I_{dss} for GaAs FETs. Probably the most promising solution is to ion-implant the active layer into the buffer layer. This should certainly eliminate any problems related to the interface. Some of the lowest noise figures for GaAs are being obtained by ion implantation.[67]

Efforts were made to thin the channel and raise the channel doping, but as described in Sec. 4.3.1, the gate sputter etch needed to get the Pt to stick removed enough material to result

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A P P E N D I X A

DOES THE DOPING FALL-OFF GIVE A TAIL TO THE I_d vs $\sqrt{\phi_B - V_g}$ PLOT?

If it does, then v_s may not be as bad at the interface as previously supposed.

Assuming an exponential dependence on doping, then

$$N_D = N_{D0}\left[1 - e^{-\lambda(d-x)}\right] \qquad \text{(A-1)}$$

where N_{D0} is the doping at the surface (x=0). Figure A.1 shows a doping profile along with plotted points representing the fit of Eq. (A-1) with $N_{D0} = 10^{17}$ cm^{-3}, d = 0.333 micron, and λ = 31.4 microns^{-1}. The tail in the measured doping profile at the lower doping values is probably an artifact of the measurement caused by series resistance.[68]

Substituting Eq. (A-1) into Eq. (3-8) gives

$$V_g - \phi_B = \frac{q}{\epsilon} N_{D0}\left[\frac{e^{-\lambda d}}{\lambda^2}\left(1 - e^{\lambda w} + \lambda w e^{\lambda w}\right) - \frac{w^2}{2}\right] . \qquad \text{(A-2)}$$

Assuming a constant v_s across the channel, substitution of Eq. (A-1) into Eq. (3-1) gives

$$I_d = qZv_s \frac{N_{D0}}{\lambda}\left[\lambda(d-w) + e^{-\lambda(d-w)} - 1\right] . \qquad \text{(A-3)}$$

Substitution of particular values of w into Eqs. (A-2) and (A-3) gives $V_g - \phi_B$ and its corresponding value of I_d. Figure A.2 shows the plot of I_d normalized by qZv_sN_{D0}/λ vs $\sqrt{\phi_B - V_g}$, revealing a straight line clear to pinch-off. It thus appears that the tail in the I_d vs $\sqrt{\phi_B - V_g}$ plots is not the result of the doping profile.

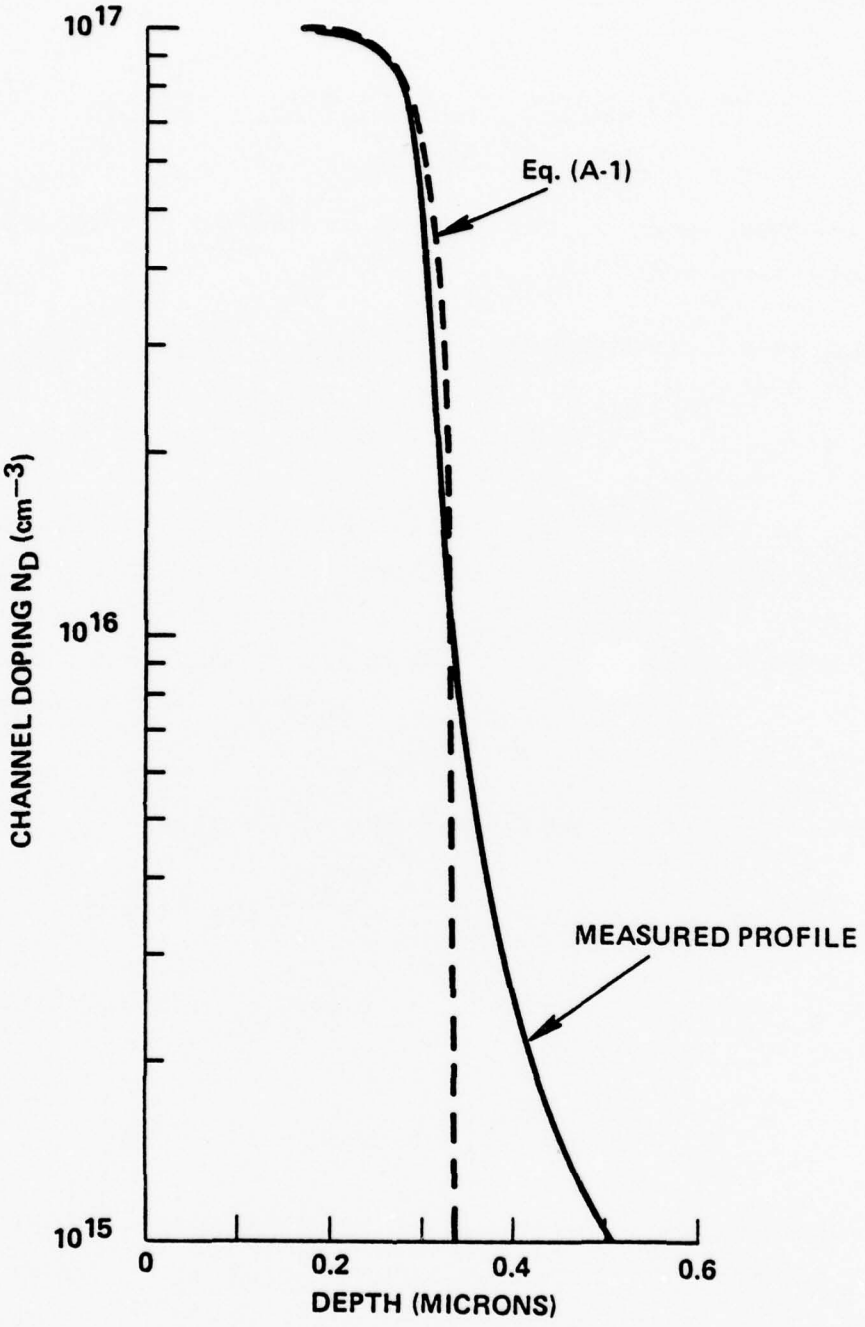


Figure A.1. Measured doping profile and Eq. (A-1) fit.

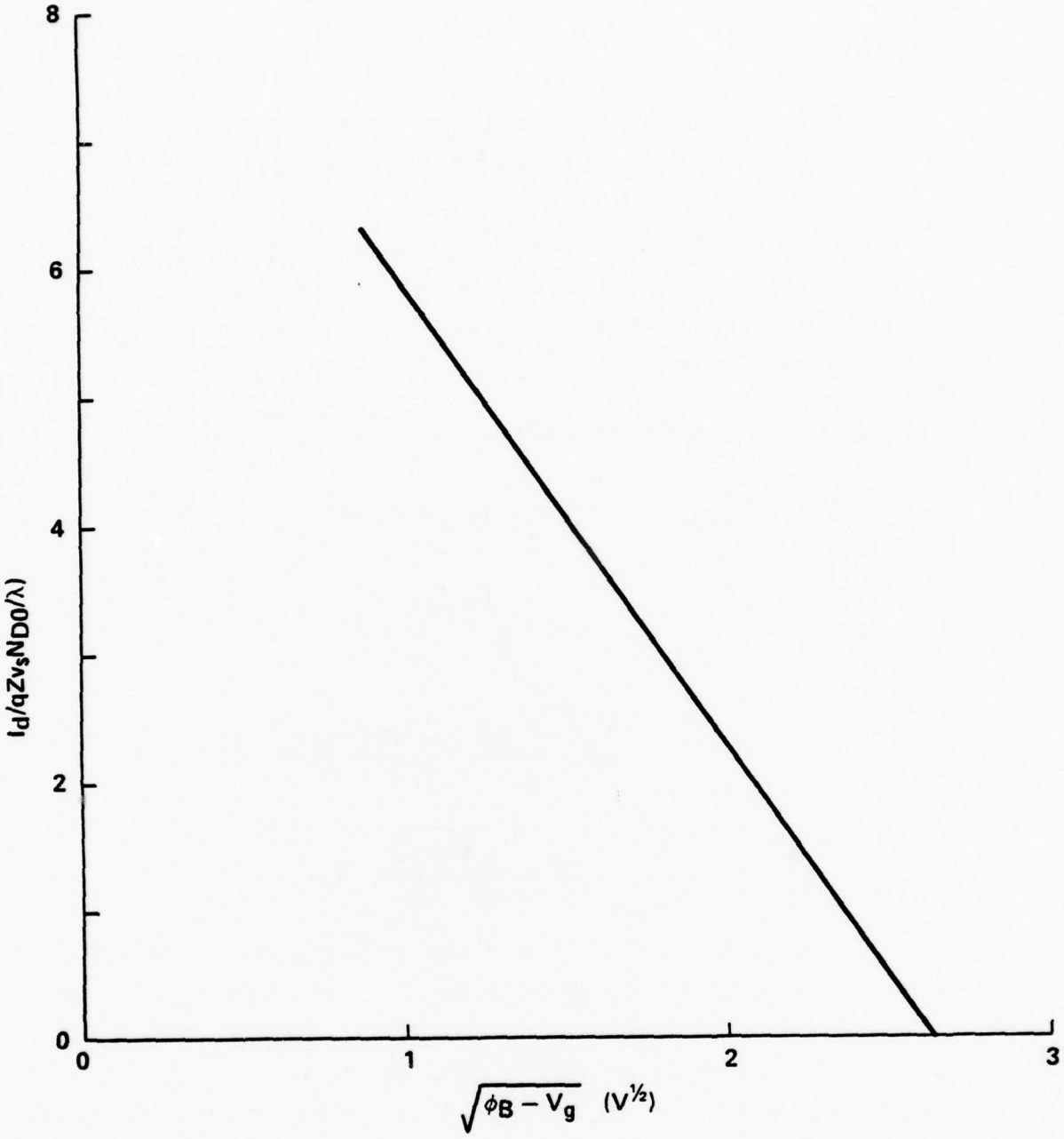


Fig. A.2. Effect of doping tail on pinch-off characteristic.

APPENDIX B

DOES THE FET FALL OUT OF SATURATION AS PINCH-OFF IS APPROACHED?

Could it be that the tail of the I_d vs $\sqrt{\phi_B - V_g}$ plot is related to the fact that, even though the device may be considered completely velocity saturated at $V_g = 0$, cannot be so considered as V_g approaches pinch-off?

Using the theory of Turner and Wilson,[40]

$$I_d = qN_D v_s Z d(1-u) \quad , \tag{B-1}$$

$$u = \sqrt{\frac{V_d + \phi_B - V_g}{V_p}} \quad , \tag{B-2}$$

$$\frac{3E_s L}{V_p} = \frac{3u^2 - 2u^3 - 3t^2 + 2t^3}{1-u} \quad , \tag{B-3}$$

$$t = \sqrt{\frac{\phi_B - V_g}{V_p}} \quad . \tag{B-4}$$

As an example, with $V_p = 7.4$ V, $E_s = 3.5 \times 10^3$ V/cm and $L = 1.0$ micron, for a given value of $\phi_B - V_g$, t is given by Eq. (B-4), u by Eq. (B-3), and then I_d by Eq. (B-1). Figure B.1 shows the resulting plot of I_d vs $\sqrt{\phi_B - V_g}$, which shows that there is a slight tail, but not significantly so. For complete velocity saturation, $u = t$. Since $t \leq u \leq 1$, then by the fact that there is a slight tail, u becomes closer to t as pinch-off is approached so that the FET becomes more saturated (not less) at pinch-off.

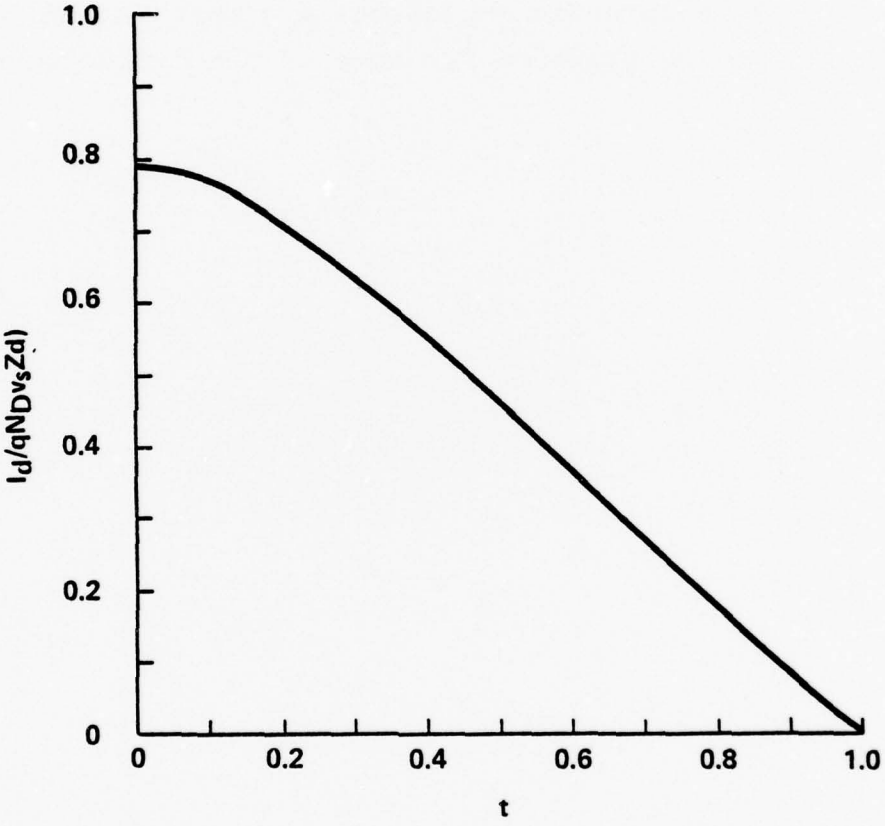


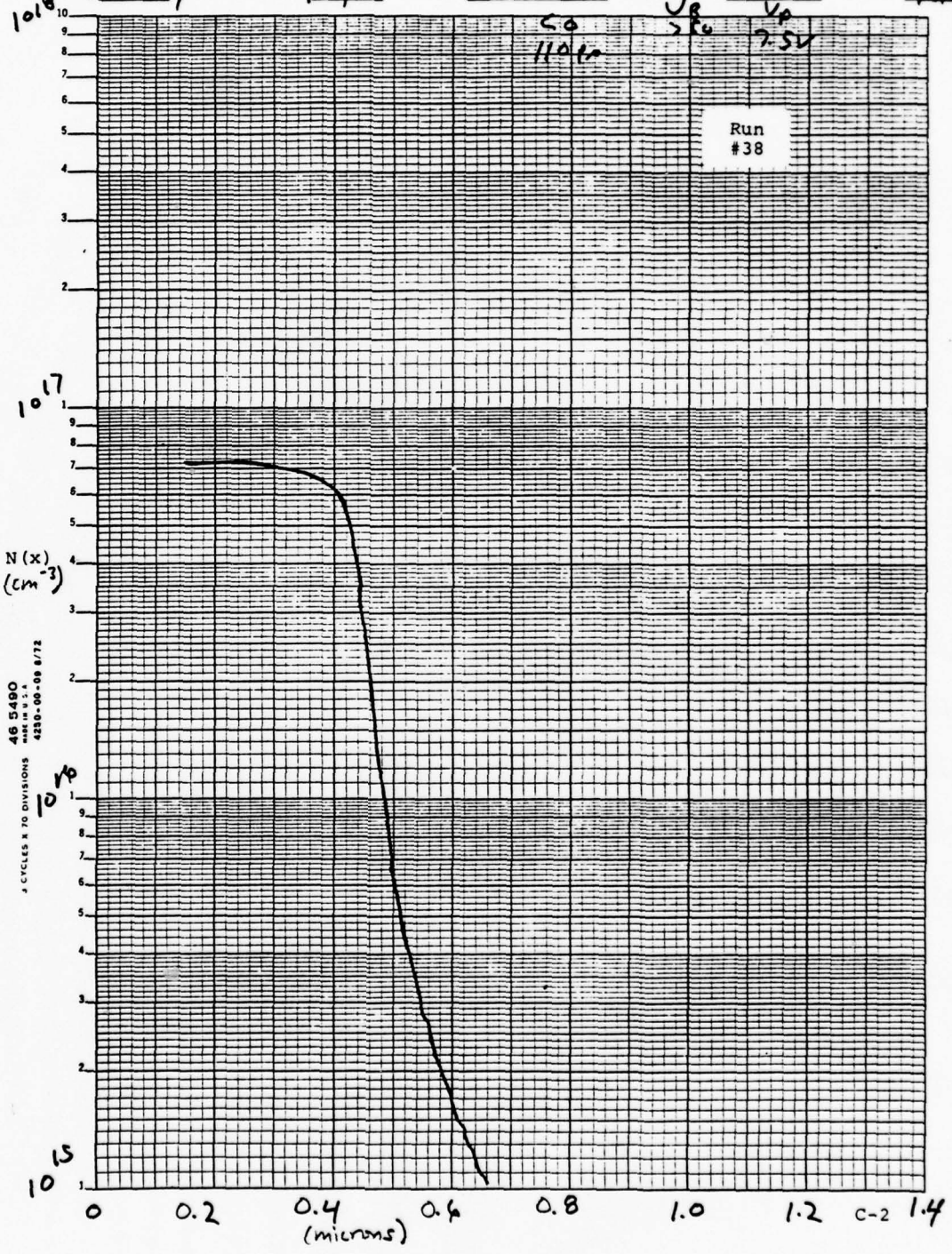
Figure B.1. Pinch-off characteristic using the theory of Turner and Wilson (Ref. 40).

APPENDIX C

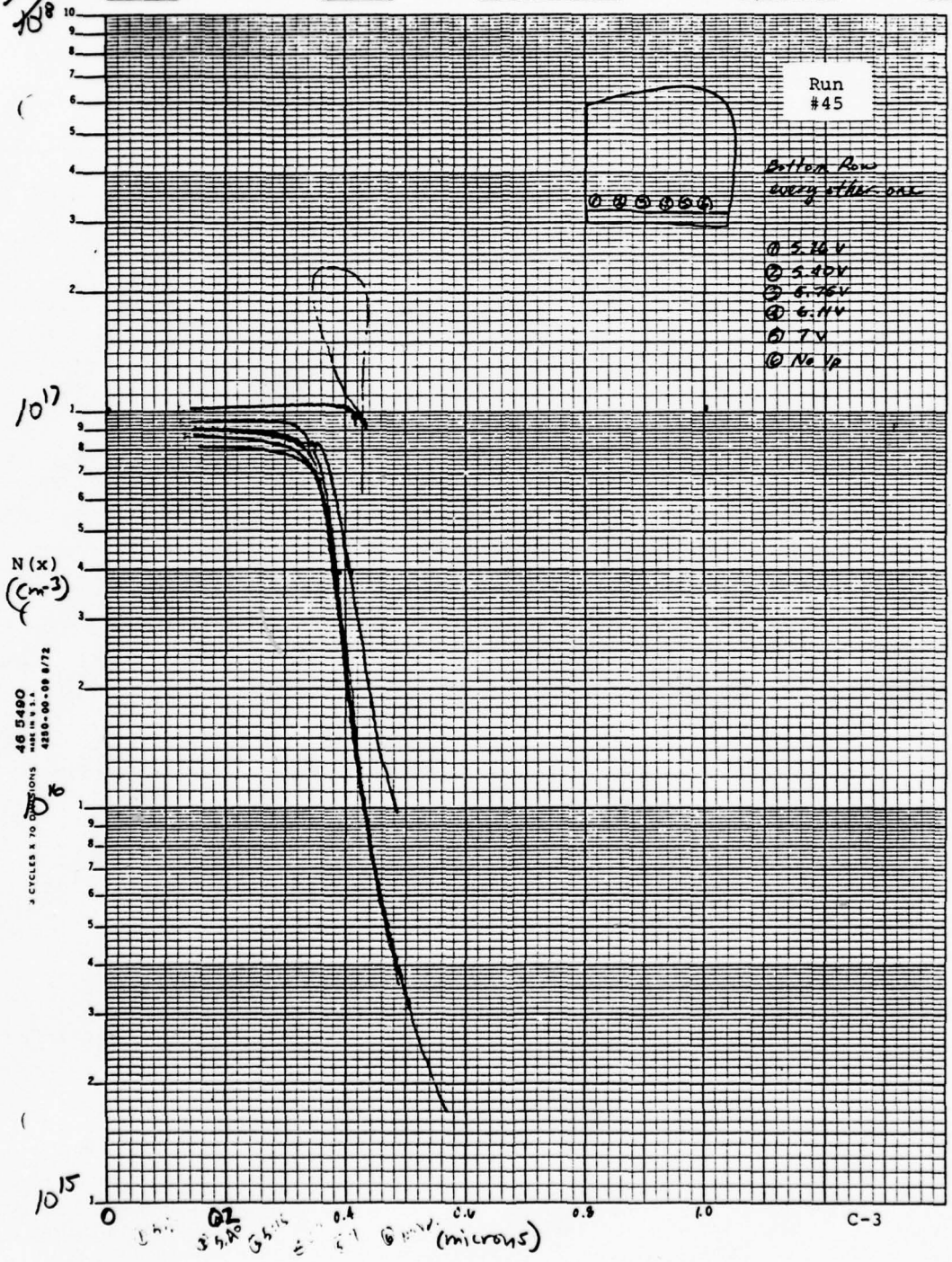
This appendix represents a compendium of doping profiles for some of the device runs.

RUN NO. TR25-14T, DIODE NO. 10,14 AREA 20.1 BARRIER 1m DATE 2/7/25

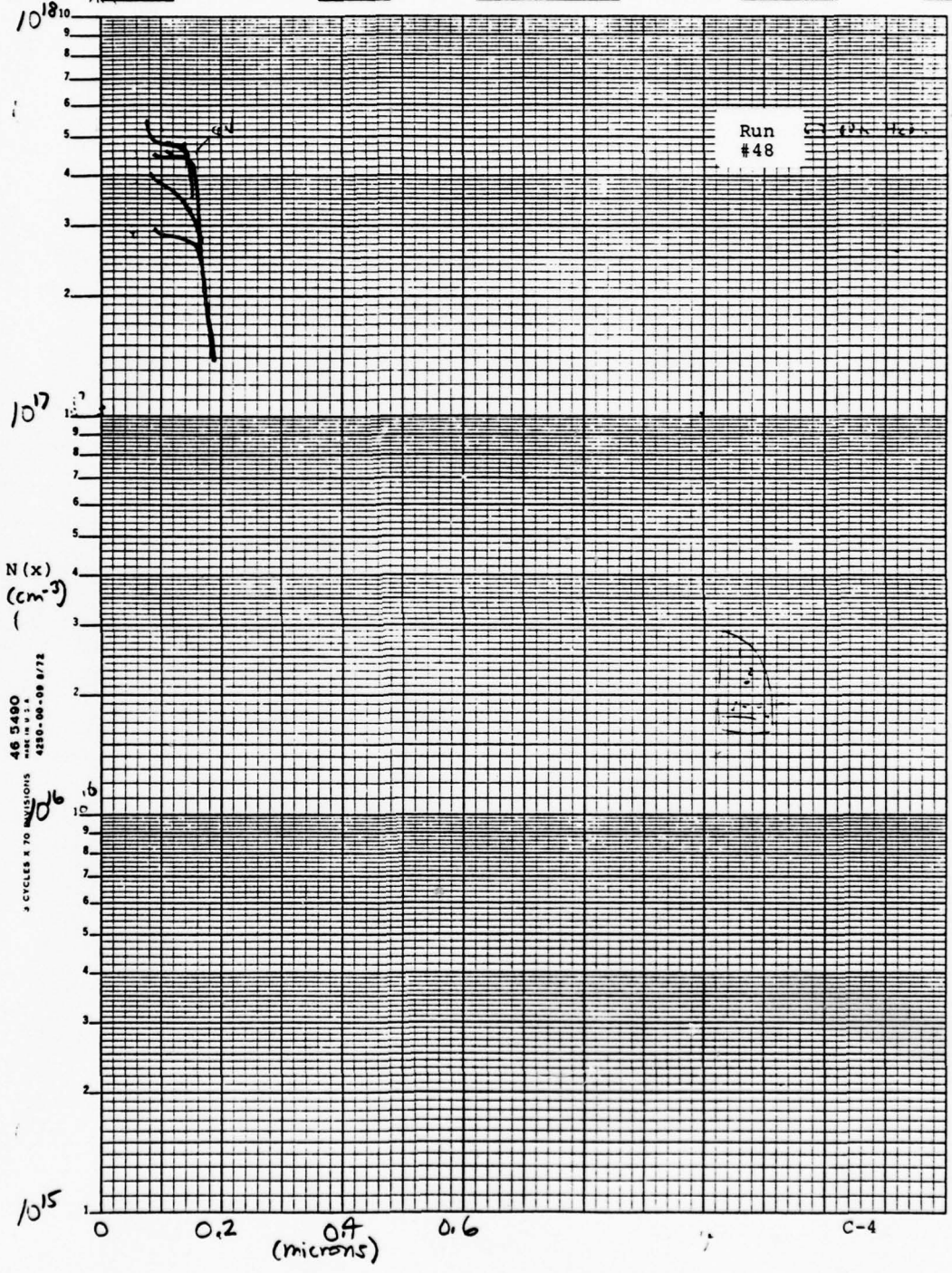
V_R < 0
V_R > V_P
V_P 2.5V
110 Å



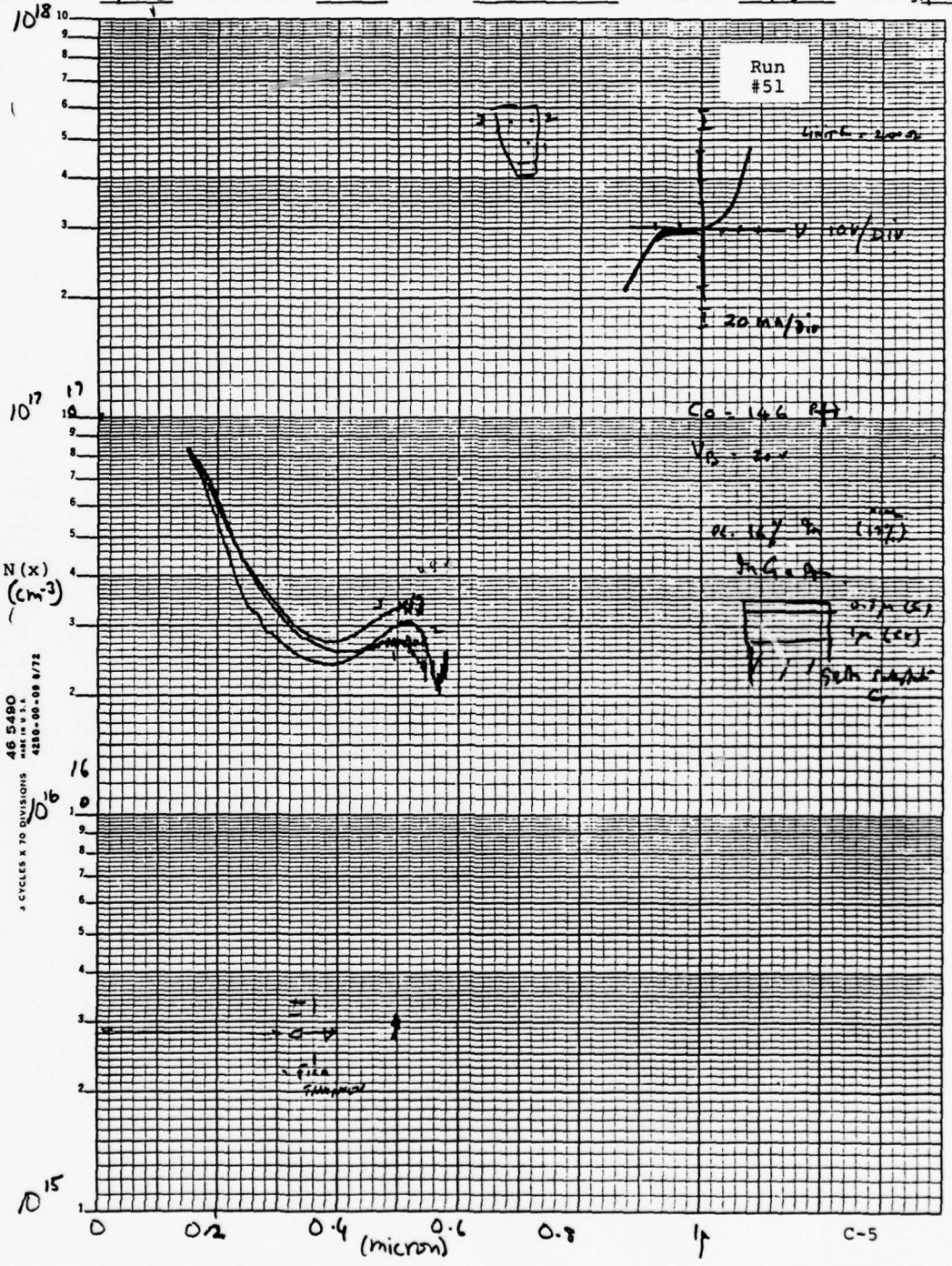
RUN NO. TR 25-16 T3 DIODE NO. InGaAs AREA ~ 20mil BARRIER Au DATE 3/31/75



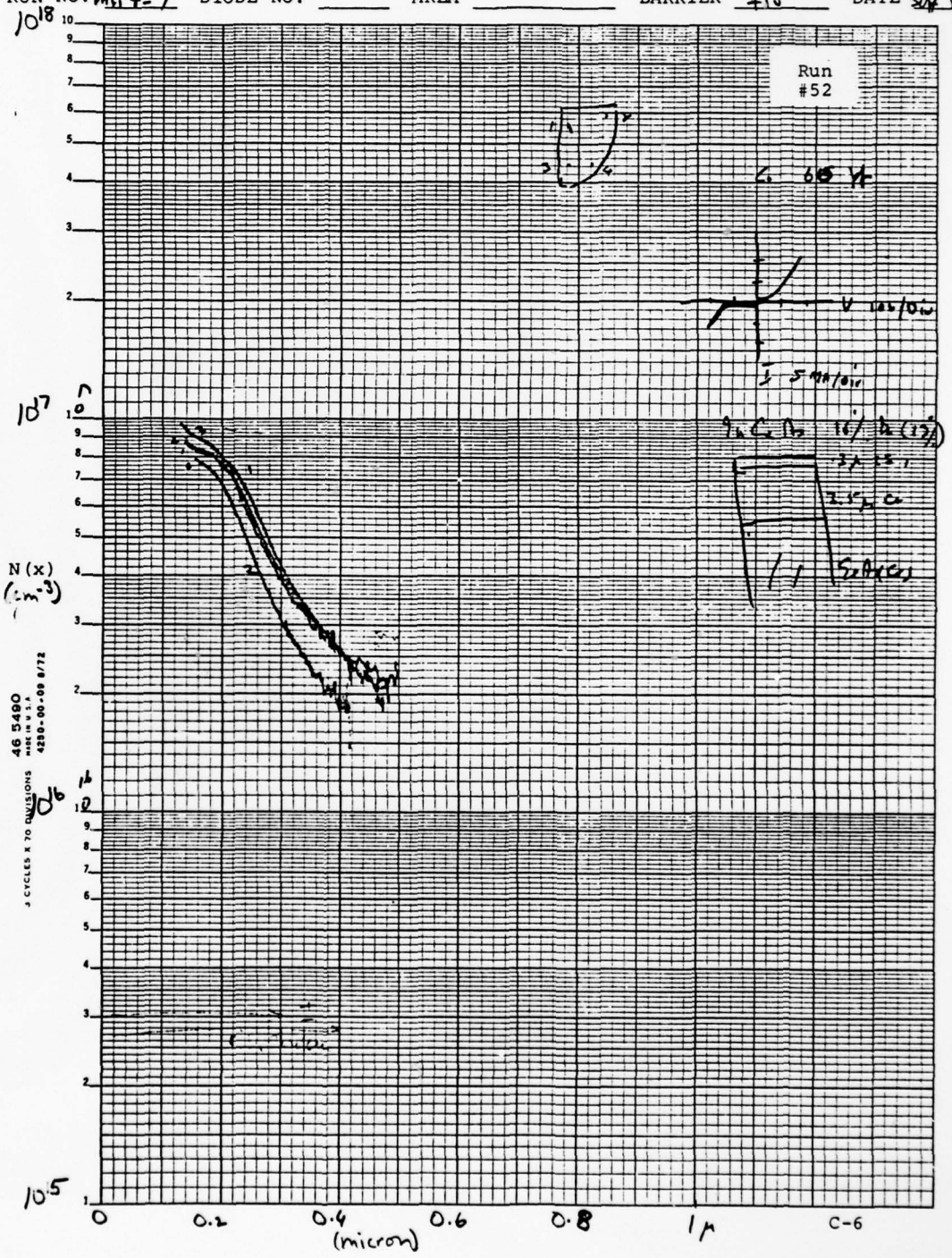
RUN NO. 43-21 DIODE NO. _____ AREA _____ BARRIER _____ DATE 7/31/74



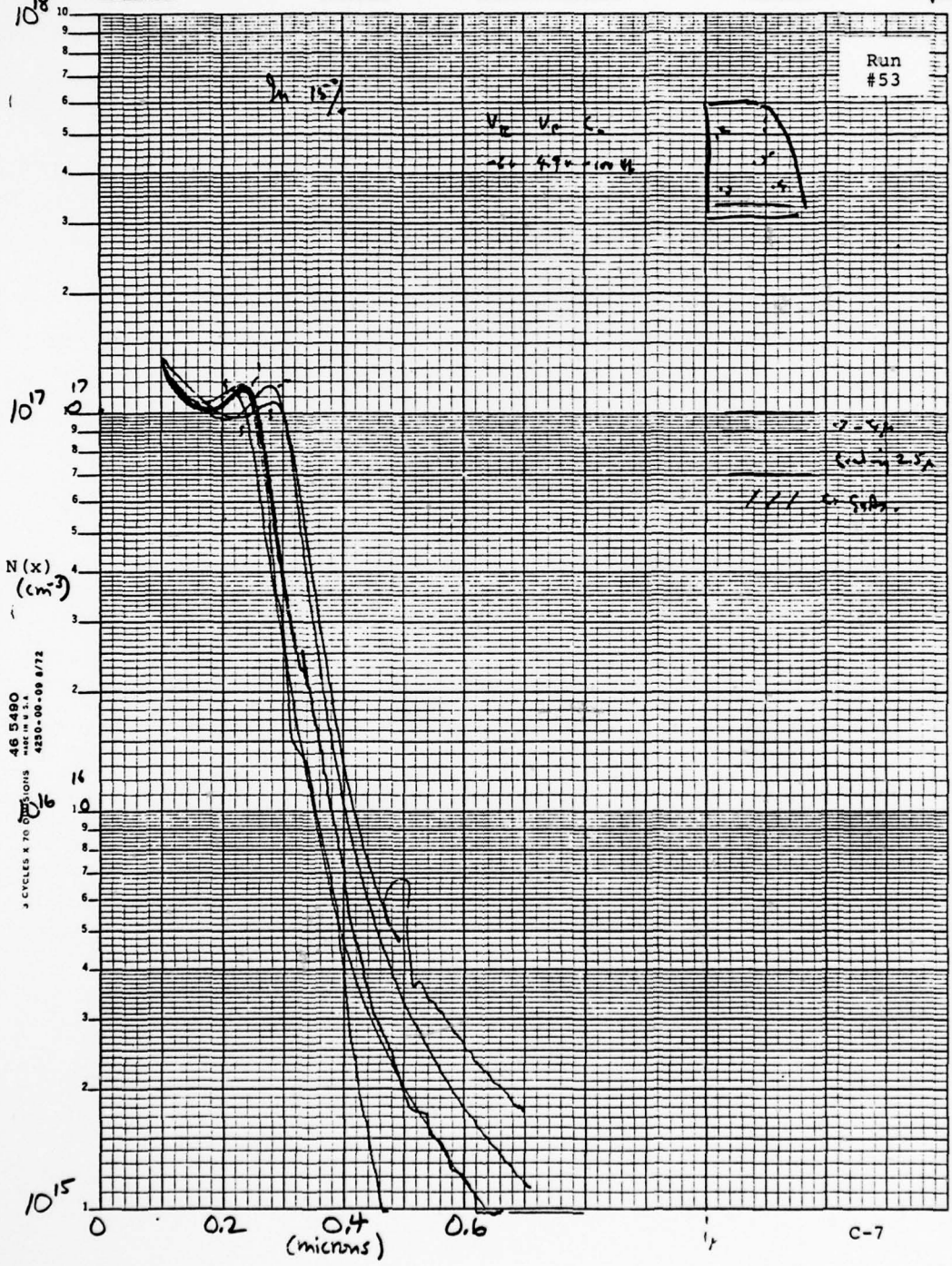
RUN NO. InC.4.6 DIODE NO. _____ AREA _____ BARRIER Au DATE Sept. 12, 197-



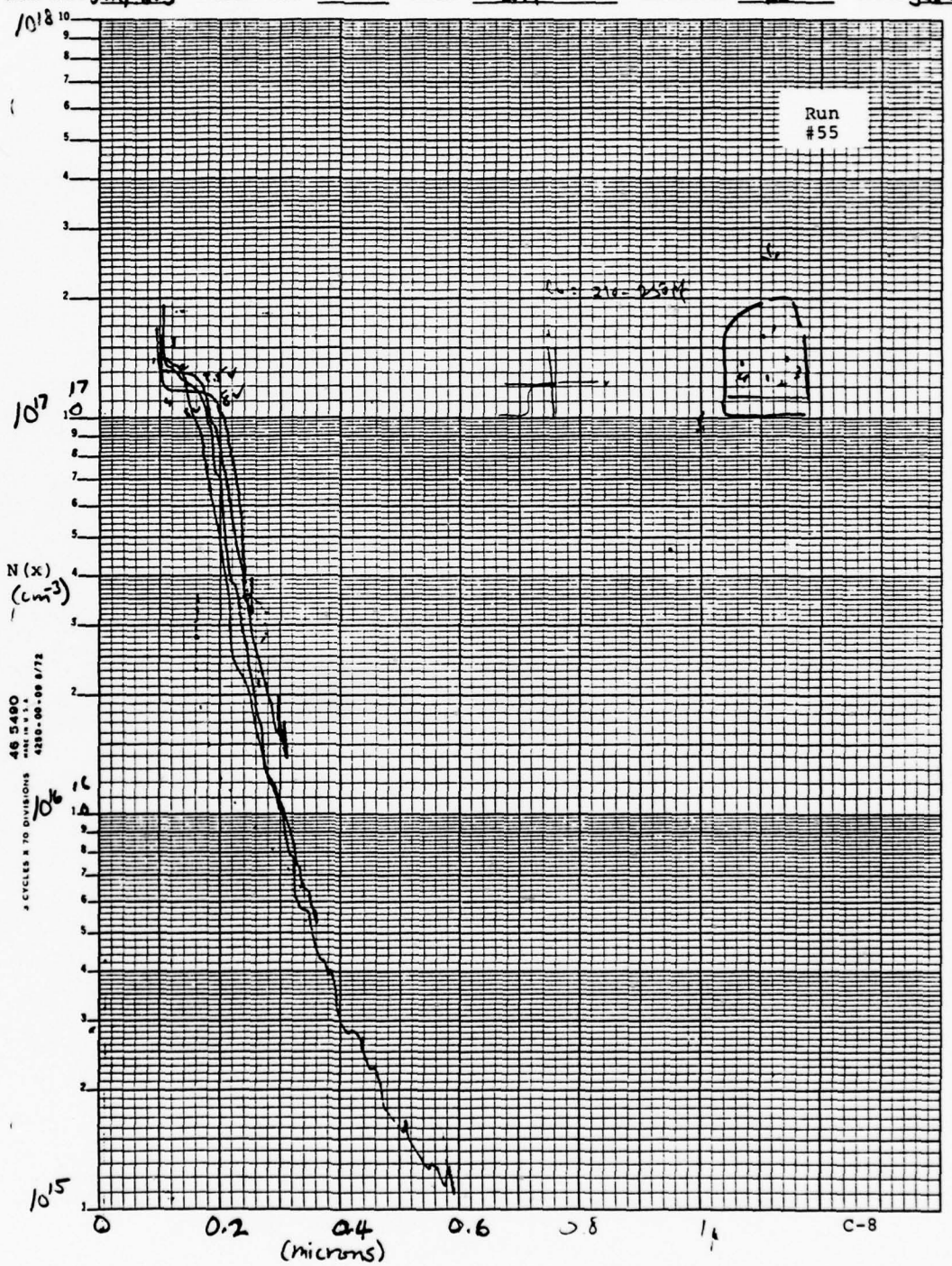
RUN NO. 9n64-7 DIODE NO. _____ AREA _____ BARRIER Au DATE 5/4 12/19



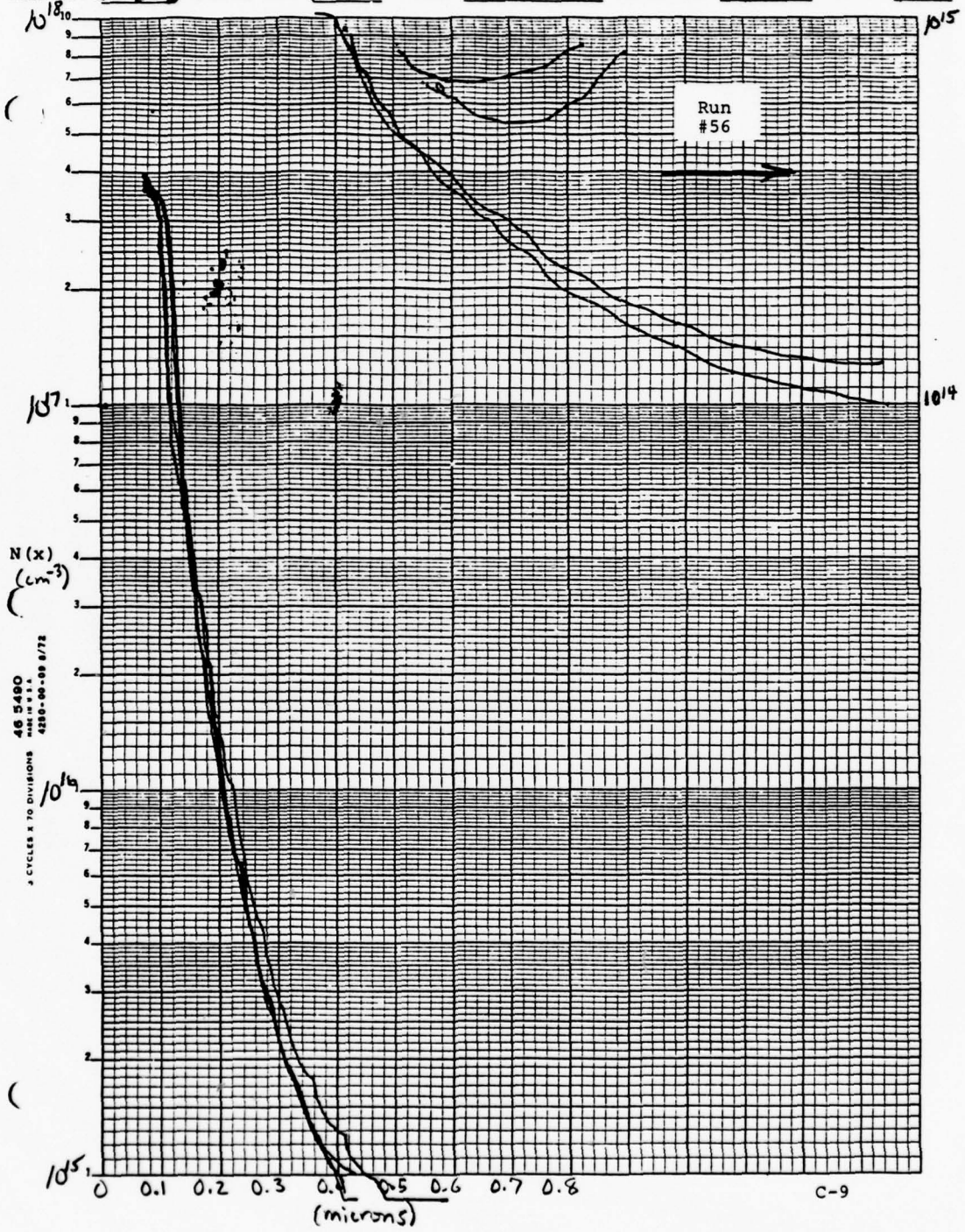
RUN NO. JnG.4-11 DIODE NO. _____ AREA _____ BARRIER Au DATE 6/22



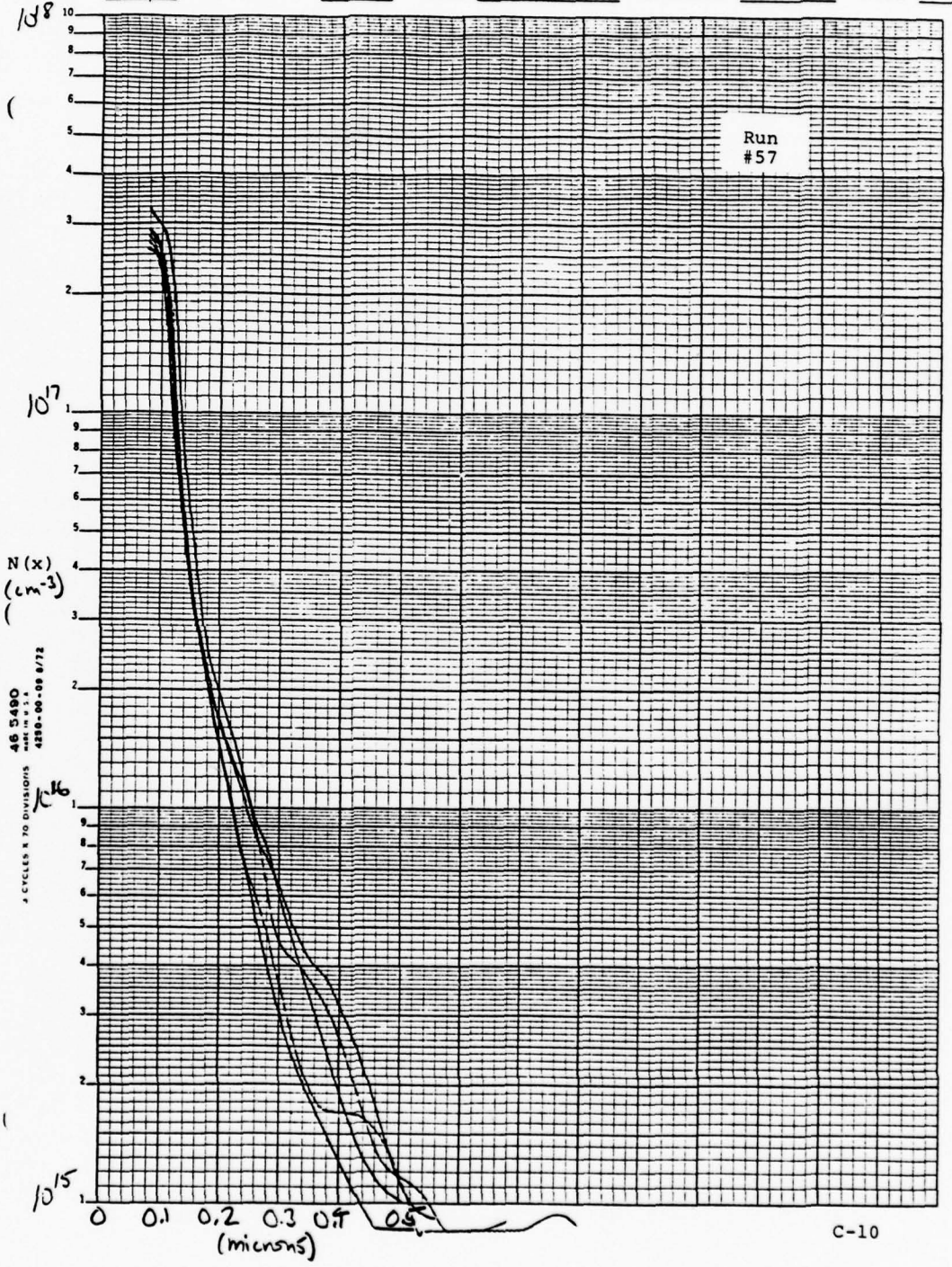
RUN NO. InG 6.3 DIODE NO. _____ AREA 2.1 BARRIER Au DATE Jan 27 '77



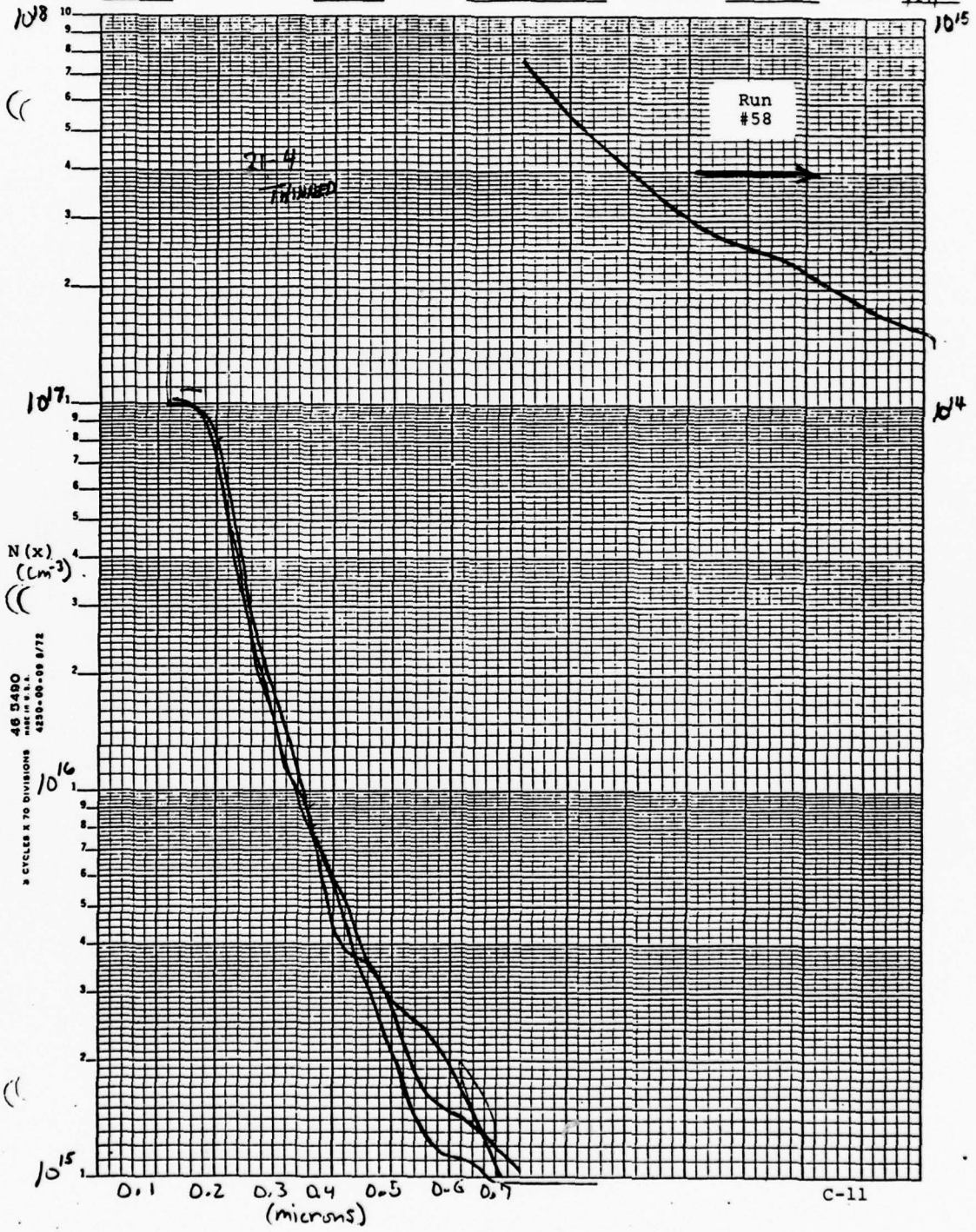
RUN NO. I-6 ~~20-5~~ DIODE NO. VARIOUS AREA 19.5 MILS D.A. BARRIER Au DATE 3/30/77



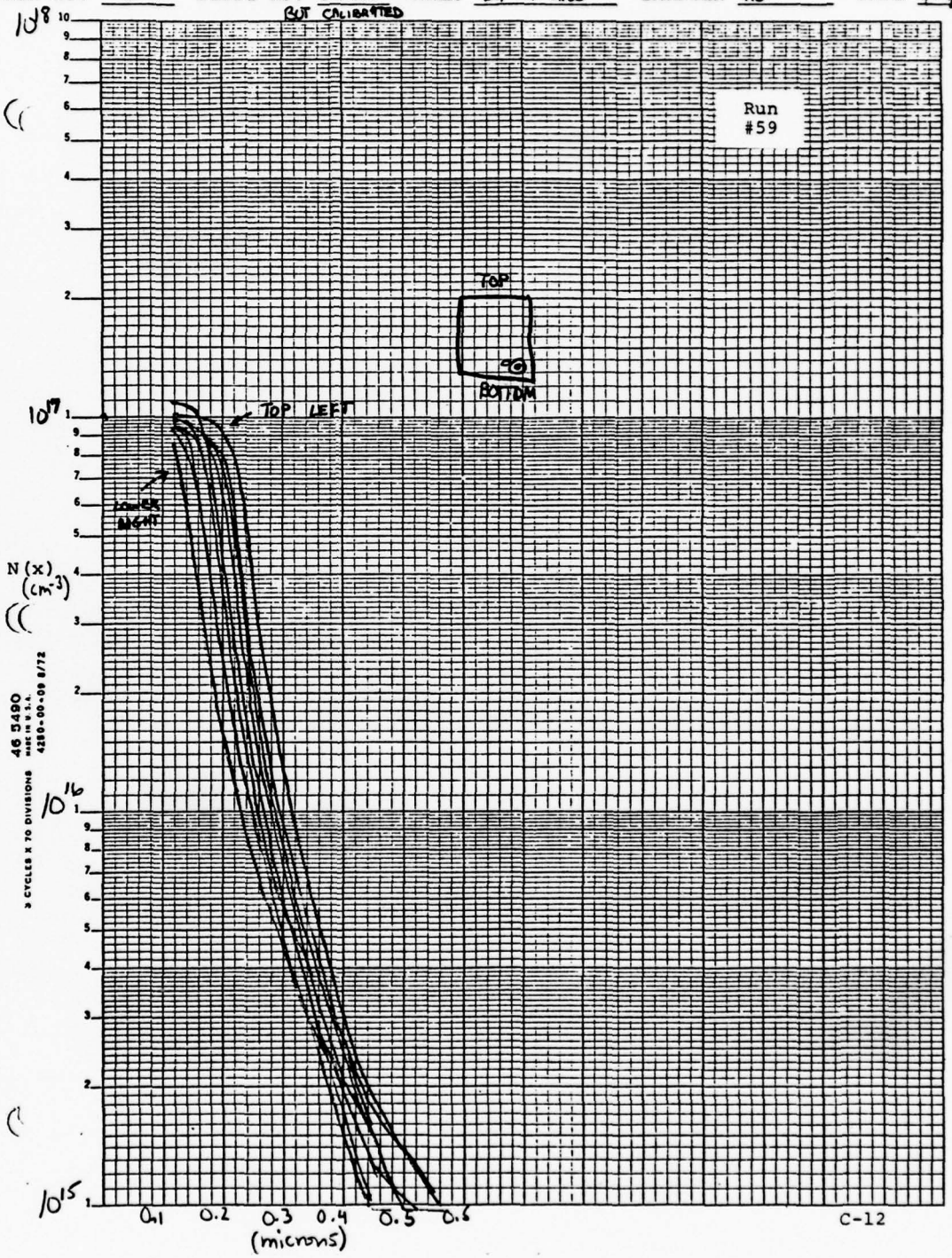
RUN NO. 20-7 DIODE NO. _____ AREA _____ BARRIER _____ DATE _____



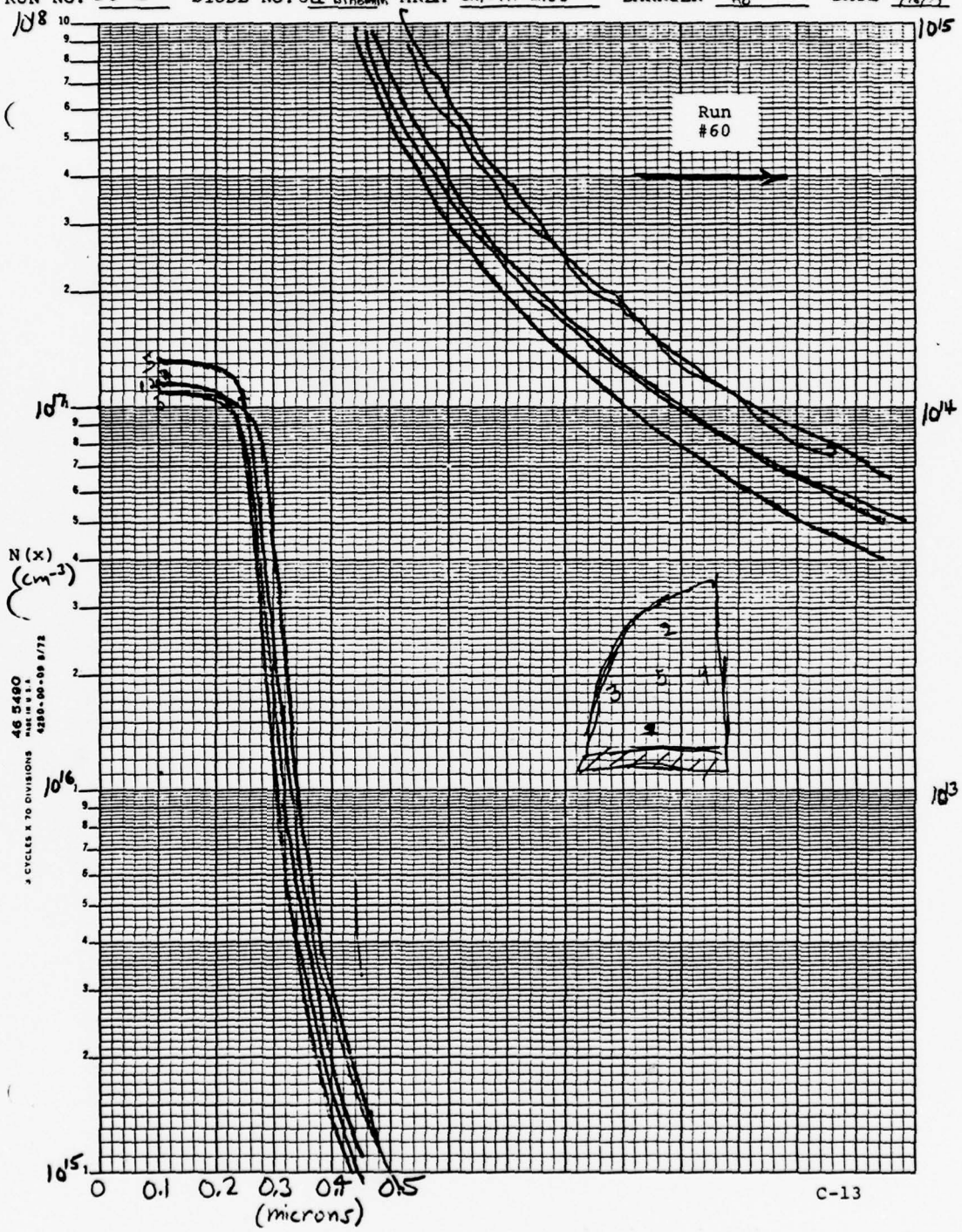
RUN NO. 21-4 DIODE NO. VARIOUS AREA _____ BARRIER flo DATE 9/27/72



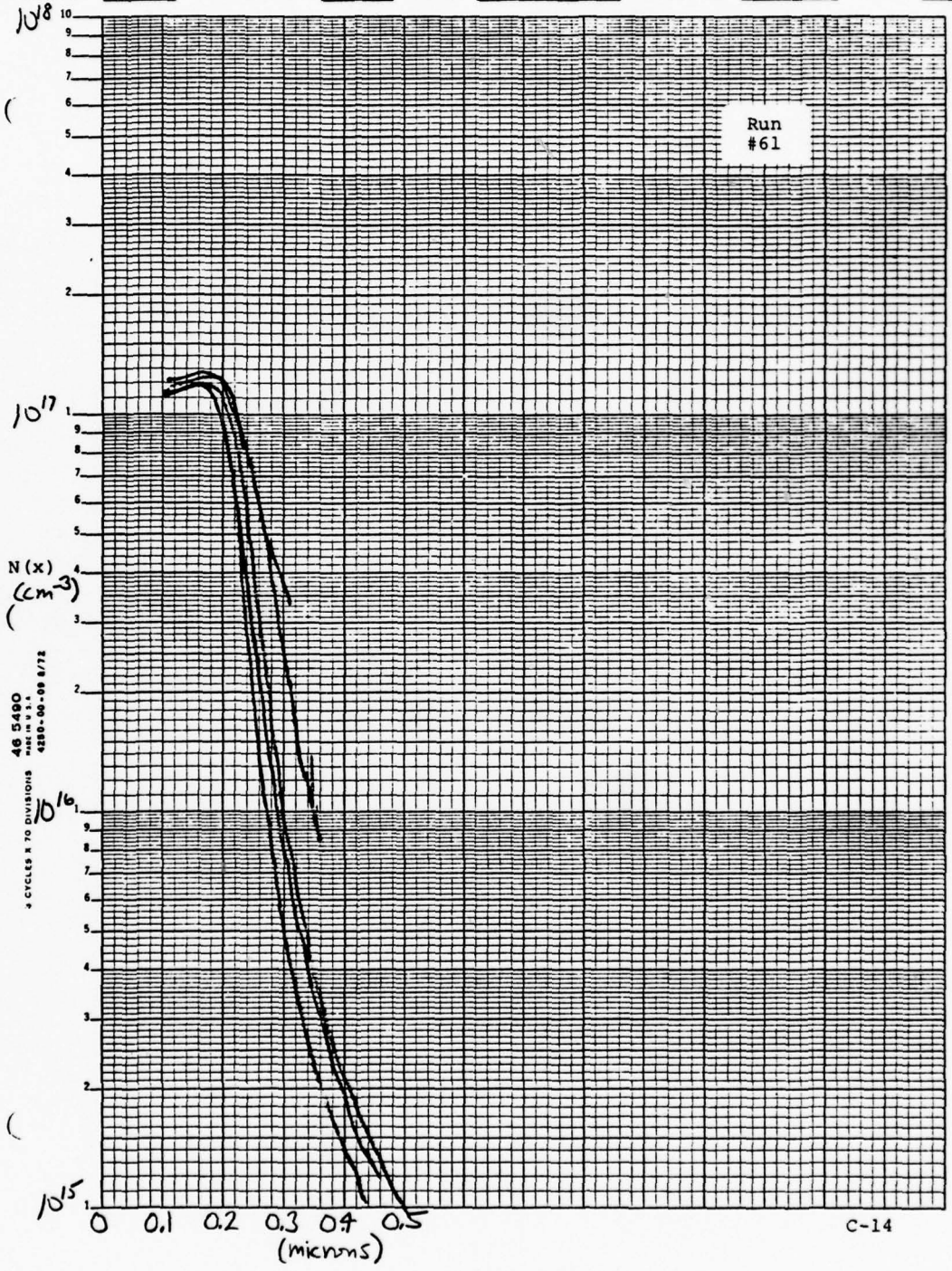
RUN NO. 21-5 DIODE NO. VARIOUS ~~AREA~~ BUT CALIBRATED DIA = 19.7 MILS BARRIER Au DATE 9/22/77



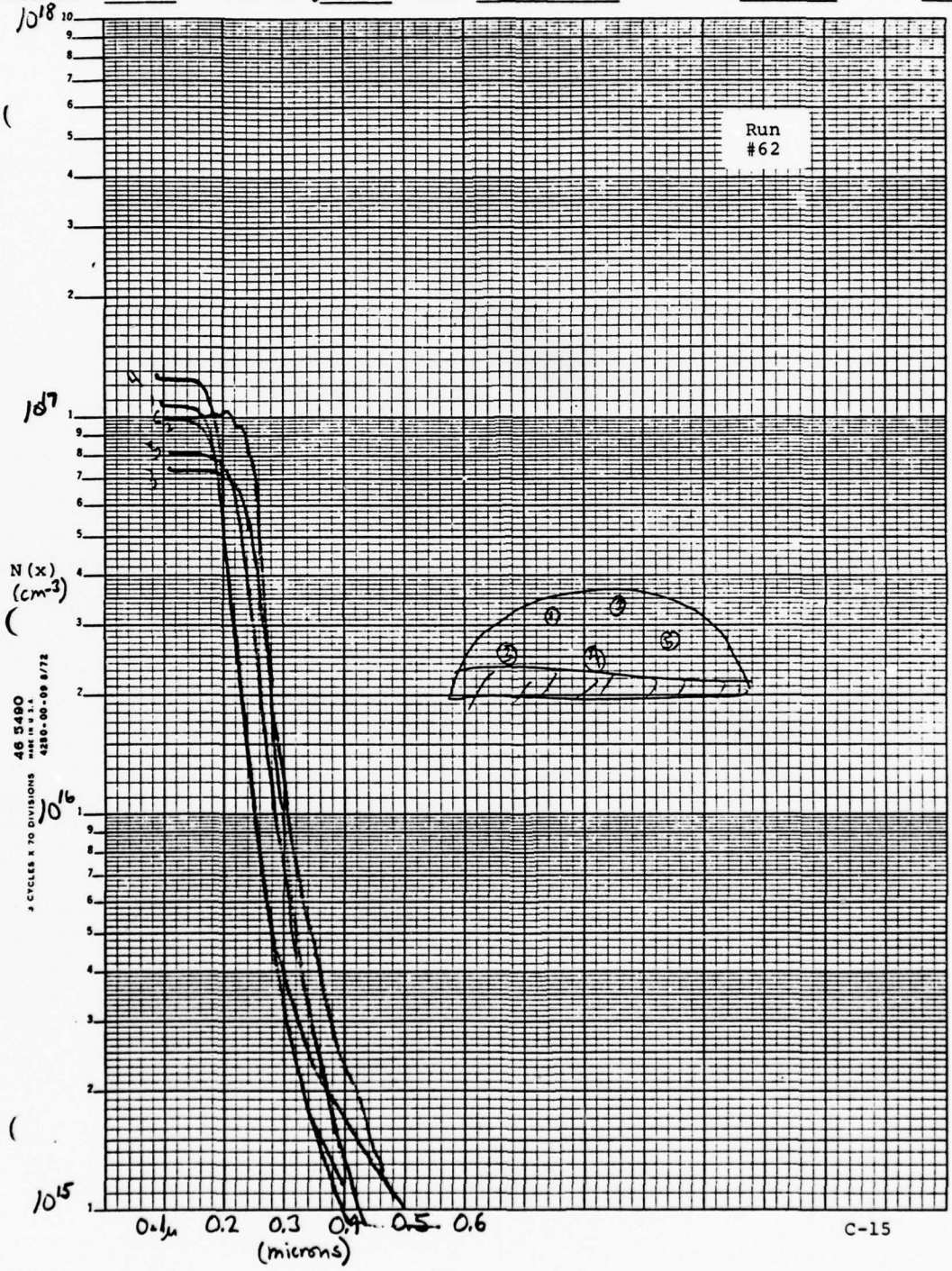
RUN NO. 23-2 DIODE NO. See diagram ~~AREA~~ DIA = 19.7 MILS BARRIER Au DATE 9/15/72



RUN NO. 23-9 DIODE NO. _____ AREA _____ BARRIER _____ DATE _____



RUN NO. In6 24-6 DIODE NO. VARIOUS DIA ~~AREA~~ 19.5 MIL BARRIER Au DATE



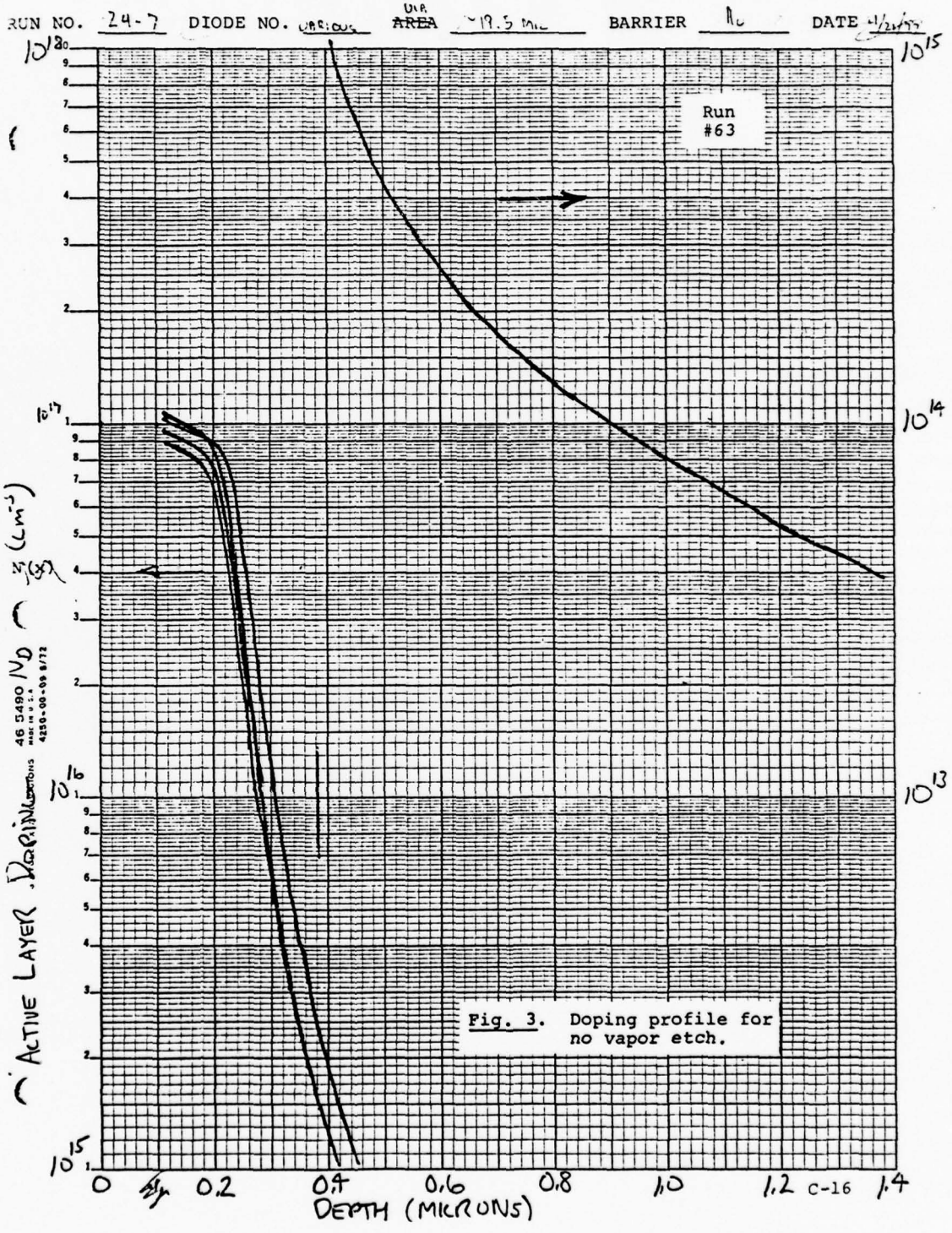


Fig. 3. Doping profile for no vapor etch.

A P P E N D I X D

This appendix represents a compendium of y-parameter data for some of the devices.

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FROM COPY FURNISHED TO DDC

F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.265	2.312	-.002	-.163	6.885	-1.237	.971	.804,
3.00	.089	3.247	-.003	-.240	6.575	-1.763	.679	1.038,
4.00	-.167	5.188	.065	-.326	7.047	-1.038	.397	2.241,
5.00	.227	7.000	.061	-.380	7.065	-1.983	.696	3.277,
6.00	.656	8.961	.086	-.450	7.797	-2.847	.934	4.273,
7.00	.955	11.037	.110	-.466	8.318	-3.170	.923	5.280,
8.00	1.538	13.653	.160	-.448	9.023	-4.397	1.000	6.328,
9.00	2.155	16.814	.243	-.440	10.503	-5.146	.821	7.686,
10.00	2.572	22.735	.340	-.326	12.030	-5.551	.471	10.739,
11.00	5.309	50.248	.816	-.238	29.915	-4.763	-.292	25.497,
12.00	4.471	2.629	.070	-.110	-.754	-6.306	1.507	-1.419,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F (MAX),
	2.00	16.505	.6416	0.000	16.335	13.37,
	3.00	21.633	.3441	0.000	14.534	36.21,
EG	4.00	13.725	-.1055	0.000	13.306	19.42,
EG	5.00	16.718	.2256	0.000	12.801	34.27,
EG	6.00	24.772	.4839	0.000	12.584	$$$$$,
EG	7.00	27.195	.5451	0.000	12.696	$$$$$,
	8.00	24.118	.7535	0.000	13.240	$$$$$,
EG	9.00	16.106	.5535	0.000	13.666	57.49,
EG	10.00	11.536	.0232	0.000	14.490	37.74,
EG	11.00	9.218	$$$$$$	0.000	15.520	31.79,
	12.00	1.579	$$$$$$	1.521	0.000	14.39,

Run #38-2

F(GHZ	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	-.358	3.289	.010	-.192	8.968	-.999	.084	1.797,
3.00	-.529	4.298	.015	-.281	9.318	-1.706	-.229	1.721,
4.00	.061	6.222	.013	-.282	9.600	-2.684	.213	2.800,
5.00	.269	8.661	.067	-.446	10.377	-3.457	.107	3.918,
6.00	.614	11.967	.130	-.530	11.409	-4.883	.167	5.544,
7.00	1.976	13.859	.090	-.665	12.246	-7.254	.552	5.714,
8.00	1.937	14.568	.191	-.405	9.600	-6.236	.502	6.204,
9.00	3.086	18.759	.196	-.377	9.926	-7.277	.483	7.942,
10.00	4.911	21.505	.413	-.340	13.048	-10.225	.574	8.478,
11.00	7.120	22.460	.526	-.370	11.965	-14.591	1.563	8.701,
12.00	8.254	26.849	.562	-.237	9.097	-14.395	1.617	12.214,
13.00	21.076	27.602	.452	-.482	2.279	-20.691	4.346	12.934,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F(MAX),
NEG	2.00	22.360	.0258	0.000	16.706	26.24,
EG	3.00	30.801	.2185	0.000	15.273	$$$$$,
EG	4.00	23.580	.2355	0.000	15.477	60.40,
NEG	5.00	16.394	.1844	0.000	13.844	33.01,
NEG	6.00	14.222	.1931	0.000	13.569	30.85,
NEG	7.00	38.105	.6185	0.000	13.265	$$$$$,
NEG	8.00	15.516	.5146	0.000	14.078	47.74,
EG	9.00	18.931	.7227	0.000	14.622	79.58,
EG	10.00	13.979	.4195	0.000	14.910	50.00,
	11.00	12.366	1.7589	9.612	0.000	45.68,
	12.00	9.189	2.4064	7.836	0.000	34.57,
	13.00	.556	$$$$$$	.527	0.000	13.86,

Run #38-3

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.823	2.276	-.019	-.183	6.169	-1.761	1.204	1.197,
3.00	.048	3.321	-.012	-.254	5.543	-1.907	.349	1.687,
4.00	.040	5.143	.008	-.322	5.569	-2.144	.134	2.849,
5.00	.467	6.974	.040	-.396	5.953	-2.438	.364	4.031,
6.00	.897	7.133	.005	-.424	5.382	-3.839	.531	3.587,
7.00	1.265	11.216	.082	-.505	6.481	-3.822	.452	6.485,
8.00	1.926	13.941	.093	-.495	6.936	-4.595	.618	7.853,
9.00	3.026	17.386	.167	-.462	7.038	-5.343	.475	9.536,
10.00	4.338	23.785	.301	-.252	9.864	-6.056	.271	13.104,
11.00	7.696	48.351	.906	-.410	18.788	-12.914	-.525	30.210,
12.00	2.023	1.301	.025	-.101	-1.556	-3.233	.424	-1.686,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F (MAX),
	2.00	9.641	2.0507	9.581	0.000	6.07,
	3.00	19.983	.3929	0.000	13.626	29.94,
NEG	4.00	23.200	.3406	0.000	12.683	57.82,
NEG	5.00	21.610	.4171	0.000	12.081	60.18,
	6.00	13.546	.9105	0.000	11.930	28.54,
	7.00	25.121	.6606	0.000	11.677	$$$$$,
	8.00	14.657	.9569	0.000	12.182	43.24,
	9.00	18.294	.9606	0.000	12.550	73.95,
NEG	10.00	12.421	.2001	0.000	14.700	41.79,
NEG	11.00	7.524	-.8739	0.000	13.606	26.16,
	12.00	5.363	5.5925	4.948	0.000	22.25,

Run #38-16

F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.442	5.277	.037	-.221	10.453	.129	.827	3.628,
3.00	.076	5.924	.047	-.294	9.980	-.950	.594	3.489,
4.00	.316	7.983	.091	-.399	10.525	-1.391	.493	4.583,
5.00	.727	10.273	.151	-.472	11.140	-1.749	.549	5.764,
6.00	-1.450	-28.169	-1.080	.372	-19.341	-20.682	-1.269	-28.013,
7.00	1.864	15.432	.214	-.623	13.136	-4.042	.630	7.711,
8.00	3.211	19.220	.300	-.507	14.830	-6.504	.652	8.998,
9.00	4.233	24.042	.443	-.502	17.552	-7.209	.720	10.722,
10.00	6.486	32.857	.807	-.702	28.225	-9.812	-.141	18.753,
11.00	17.173	82.555	2.322	-.479	73.462	-18.723	-.610	40.702,
12.00	3.828	4.557	.112	-.188	-2.854	-7.428	.333	-.750,
13.00	10.399	22.607	.629	-.271	7.040	-15.610	.211	8.010,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F (MAX),
NEG	2.00	30.306	.1329	0.000	16.678	65.51,
NEG	3.00	17.629	-.0344	0.000	15.268	22.83,
NEG	4.00	15.317	-.0221	0.000	14.134	23.33,
NEG	5.00	13.759	-.0111	0.000	13.567	24.37,
NEG	6.00	10.082	-.7700	0.000	13.941	19.15,
NEG	7.00	14.378	.2280	0.000	13.193	36.64,
NEG	8.00	14.181	.3176	0.000	14.392	40.94,
NEG	9.00	12.522	.1530	0.000	14.524	38.05,
NEG	10.00	9.447	-.5544	0.000	14.460	29.67,
NEG	11.00	8.721	$$$$$$	0.000	15.049	30.02,
	12.00	9.826	2.4508	8.902	0.000	37.20,
NEG	13.00	14.904	.3572	0.000	13.982	72.30,,,

Run #38-31

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

F(GHZ	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.093	4.390	.008	-.156	17.063	-2.844	.768	6.775,
3.00	.159	7.139	.007	-.232	18.219	-3.918	.492	2.982,
4.00	-13.052	35.885	.278	-.329	24.565	19.750	.966	4.259,
5.00	1.819	14.647	.099	-.368	22.767	-7.153	.664	5.595,
6.00	3.341	22.118	.179	-.425	28.173	-13.053	.804	7.767,
7.00	8.092	29.591	.220	-.493	30.891	-24.069	1.092	9.372,
8.00	6.898	31.754	.294	-.021	23.666	-18.454	.670	9.812,
9.00	18.194	46.181	.593	.004	28.175	-29.185	1.243	11.517,
10.00	38.941	55.481	1.200	.130	27.490	-55.716	1.675	11.616,
11.00	69.615	42.959	1.592	-.397	-5.502	-57.682	2.110	12.073,
12.00	71.738	24.961	1.112	-.459	-21.991	-48.178	3.288	16.565,
13.00	66.438	-4.953	.673	-.616	-38.822	-22.135	3.928	19.786,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F(MAX),
EG	2.00	30.566	.1323	0.000	20.430	67.50,
EG	3.00	22.166	.1017	0.000	18.966	43.20,
EG	4.00	11.044	$$$$$$	0.000	19.421	14.27,
EG	5.00	21.817	.3820	0.000	17.983	61.63,
EG	6.00	19.960	.4094	0.000	18.283	59.86,
	7.00	22.643	1.0751	16.936	0.000	94.90,
EG	8.00	19.777	.3022	0.000	20.085	77.97,
	9.00	16.839	1.1808	15.778	0.000	74.33,
	10.00	14.702	1.2040	14.387	0.000	54.34,
	11.00	7.277	3.4260	7.219	0.000	25.42,
	12.00	4.318	6.1345	4.335	0.000	19.71,
	13.00	3.459	$$$$$$	2.504	0.000	17.25,

Run #35A-12

F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	1.009	4.240	-.011	-.135	18.399	-4.422	1.652	1.059,
3.00	.372	6.156	.002	-.166	16.717	-4.951	.834	1.477,
4.00	.454	8.895	.032	-.202	16.606	-5.408	.617	2.587,
5.00	1.172	11.922	.074	-.270	17.824	-6.322	.868	3.792,
6.00	2.185	13.256	.010	-.196	16.431	-10.635	1.751	3.309,
7.00	3.661	19.047	.197	-.244	15.000	-15.139	5.055	2.776,
8.00	5.877	24.730	.232	-.112	22.352	-13.772	1.693	5.672,
9.00	10.214	31.335	.424	-.024	23.736	-17.625	1.344	6.662,
10.00	15.777	43.996	.829	-.024	35.400	-25.326	.837	9.636,
11.00	44.252	103.654	1.524	.561	78.950	-57.687	.759	24.070,
12.00	14.353	7.123	.280	-.112	-15.606	-14.205	.139	-2.581,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F (MAX),
	2.00	16.810	1.6095	16.871	0.000	13.85,
	3.00	24.234	.4899	0.000	20.217	48.85,
EG	4.00	24.681	.3123	0.000	19.310	68.57,
EG	5.00	24.566	.4564	0.000	18.293	84.58,
	6.00	14.130	2.4897	13.201	0.000	30.53,
	7.00	8.504	5.6530	7.326	0.000	18.63,
	8.00	15.491	2.4082	13.463	0.000	47.60,
	9.00	17.655	1.4180	14.583	0.000	68.70,
EG	10.00	14.537	-.0647	0.000	17.200	53.31,
EG	11.00	14.321	-.5386	0.000	17.795	57.21,
	12.00	12.466	1.5631	14.036	0.000	50.52,

Run #35A-16

1975

VARIAN ASSOCIATES TEST REPORT
FET

SER# 45-3
BIAS= 3.50 VOLTS, 50.00 MA

Run #45-3

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
	①	②	③	④	⑤	⑥	⑦	⑧
2000.00	.15	3.37	12.59	-1.41	.01	-.12	.39	1.20
2500.00	.23	4.16	12.86	-1.97	.01	-.14	.38	1.42
3000.00	.33	5.06	13.03	-2.54	.02	-.17	.50	1.70
3500.00	.49	5.95	13.61	-2.89	.04	-.19	.55	2.04
4000.00	.60	6.94	13.59	-3.46	.04	-.20	.55	2.31
4500.00	.74	7.95	14.22	-3.82	.05	-.22	.57	2.82
5000.00	.91	9.11	14.72	-4.29	.08	-.24	.59	3.27
5500.00	1.13	10.44	15.19	-5.39	.11	-.21	.61	3.86
6000.00	1.49	11.89	15.66	-6.30	.11	-.22	1.24	4.45
6500.00	1.90	13.27	15.59	-6.83	.15	-.25	1.15	4.00
7000.00	2.44	14.78	16.28	-7.77	.19	-.20	.83	4.70
7500.00	2.96	16.28	16.84	-8.55	.16	-.15	.97	5.21
8000.00	3.61	17.87	17.44	-9.98	.23	-.10	.94	5.52
8500.00	4.57	19.41	17.84	-10.78	.35	-.04	.86	5.98
9000.00	5.53	21.09	18.59	-12.70	.38	.05	.90	6.29
9500.00	6.52	22.94	19.53	-14.55	.41	.12	1.08	6.80
10000.00	8.34	25.19	20.34	-16.84	.64	.22	.97	7.31
10500.00	10.80	27.44	20.53	-19.28	.83	.35	.94	8.05
11000.00	13.19	29.44	19.66	-22.97	.91	.39	.80	8.22
11500.00	16.25	32.12	20.31	-26.97	1.09	.39	.53	9.19
12000.00	21.50	33.87	18.84	-32.44	1.38	.38	.34	9.41
12500.00	27.56	34.50	14.84	-37.81	1.49	.44	.22	10.02
13000.00	35.25	33.06	9.00	-43.56	1.57	.25	-.24	10.89
13500.00	43.75	26.28	-3.74	-47.31	1.45	.05	-.83	11.87
14000.00	48.37	13.84	-17.34	-45.81	.78	.55	-.28	14.08
14500.00	44.50	1.67	-29.00	-30.84	.18	2.48	1.90	16.59
15000.00	52.12	5.77	-11.73	-20.47	9.81	10.34	14.59	13.70
15500.00	29.50	-29.31	-36.69	-18.50	4.84	-8.09	-1.56	7.33
16000.00	15.23	-21.69	-31.56	-3.97	.83	-4.55	-1.08	11.45

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	1.7	.10	28.0	15.2	13.3	289.1	11.2	222.3	711.7
2500.00	1.8	.18	26.3	13.5	13.2	234.4	11.0	167.8	617.2
3000.00	1.8	.20	23.9	12.0	12.7	192.4	10.0	149.0	510.2
3500.00	2.0	.21	22.2	10.6	13.5	163.7	9.6	118.2	432.0
4000.00	1.9	.26	21.3	9.8	12.3	140.4	9.6	95.2	389.5
4500.00	2.1	.31	20.6	9.1	11.5	122.1	9.4	68.4	323.8
5000.00	2.2	.22	20.0	8.5	10.6	106.6	9.3	52.7	281.6
5500.00	2.3	.21	19.5	7.9	9.9	93.1	9.3	39.5	242.6
6000.00	2.0	.78	15.6	7.0	10.2	81.4	6.6	57.1	201.2
6500.00	1.8	.73	15.0	6.4	10.2	72.7	6.8	64.6	220.7
7000.00	2.0	.47	16.0	5.8	10.4	64.9	8.2	35.6	199.0
7500.00	1.9	1.02	18.5		4.2	54.4		.8	170.1
8000.00	1.9	.80	14.8	5.0	10.3	53.3	8.0	28.4	171.1
8500.00	1.8	.28	14.9	4.5	10.8	48.4	8.6	20.6	156.9
9000.00	1.9	.21	14.9	4.2	10.8	44.2	8.8	18.2	151.2
9500.00	2.0	.40	14.1	4.0	10.6	40.3	8.1	16.4	139.1
10000.00	2.0	-.03	14.7	3.6	10.7	35.7	9.1	12.5	128.3
10500.00	1.7	-.15	14.9	3.3	11.1	31.5	9.9	8.7	116.0
11000.00	1.7	-.18	15.3	3.0	11.4	28.3	10.6	6.9	112.7
11500.00	1.8	-.41	17.8	2.9	11.2	24.7	13.1	3.1	100.4
12000.00	1.8	-.45	19.0	2.5	11.9	20.9	14.7	2.0	96.1
12500.00	1.6	-.42	19.5	2.2	12.8	17.6	15.6	1.5	90.3
13000.00	1.5	-.60		1.9	13.8	14.0		-.4	83.9
13500.00	1.4	-1.0		1.5	15.7	9.9		-2.5	78.2
14000.00	1.2	-.91		1.1	18.5	5.9		-1.6	67.7
14500.00	-.4	.92	10.9	.7	22.3	2.7	10.6	2.6	56.0
15000.00	-9.3	4.21	-7.0		18.7	6.7		28.9	36.8
15500.00	.8	.61	5.4	2.4	11.0	-12.1	2.2	66.7	92.1
16000.00	2.3	.08	11.1	2.5	13.9	-28.7	6.3	18.7	106.1

MAY 1975

VARIAN ASSOCIATES TEST REPORT
FET

SER# 45-11 39
BIAS= 3.50 VOLTS, 4.00 MA

Run
Y REAL AND IMAGINARY: #45-11

FREQ	11		21		12		22	
2000.00	.14	3.53	12.92	-1.60	.01	-.15	.78	1.21
2500.00	.23	4.35	13.14	-2.16	.00	-.18	.76	1.43
3000.00	.33	5.27	13.31	-2.73	.01	-.23	.89	1.74
3500.00	.48	6.15	13.83	-3.11	.03	-.25	.96	2.04
4000.00	.56	7.15	13.69	-3.68	.03	-.26	.94	2.30
4500.00	.68	8.17	14.22	-4.03	.04	-.30	.95	2.76
5000.00	.82	9.36	14.66	-4.46	.07	-.33	.94	3.24
5500.00	1.00	10.67	14.84	-5.48	.08	-.31	.92	3.67
6000.00	1.33	12.05	15.08	-6.01	.06	-.32	.97	4.14
6500.00	1.65	13.37	15.37	-6.66	.10	-.35	.98	4.72
7000.00	2.11	14.69	15.61	-7.52	.11	-.31	1.10	5.37
7500.00	2.41	16.03	15.91	-7.91	.12	-.20	1.15	5.70
8000.00	2.92	17.53	16.28	-9.22	.18	-.23	1.22	6.16
8500.00	3.62	18.87	16.37	-9.70	.27	-.17	1.22	6.59
9000.00	4.07	20.19	16.75	-10.94	.27	-.07	1.33	6.95
9500.00	4.62	21.94	17.37	-12.19	.27	-.07	1.49	7.35
10000.00	5.72	23.66	17.59	-13.30	.41	.02	1.36	7.91
10500.00	7.02	25.41	17.75	-14.64	.51	.17	1.43	8.62
11000.00	8.09	27.00	16.81	-16.47	.49	.23	1.32	8.78
11500.00	9.16	28.91	17.59	-18.03	.59	.26	1.15	9.92
12000.00	11.30	30.91	17.47	-20.22	.75	.40	1.10	9.86
12500.00	13.45	32.56	16.16	-22.59	.73	.57	1.10	10.69
13000.00	16.22	34.31	15.44	-25.06	.79	.59	.91	11.33
13500.00	20.09	35.31	12.73	-28.69	.90	.76	.68	11.42
14000.00	25.22	35.94	11.52	-32.25	.63	1.08	.48	13.36
14500.00	32.12	36.75	3.91	-35.06	-.12	2.27	1.28	17.34
15000.00	49.37	51.06	25.81	-25.37	6.80	11.55	22.12	17.12
15500.00	65.62	-.84	-29.41	-61.62	6.61	-5.50	-.70	4.09
16000.00	46.75	-20.19	-47.25	-30.22	2.02	-4.27	-.78	9.39

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	1.7	.18	25.5	15.4	11.5	275.8	8.3	339.8	558.6
2500.00	1.8	.29	23.4	13.3	12.7	223.8	8.3	265.6	513.3
3000.00	1.8	.36	21.4	11.9	12.2	184.0	7.7	215.2	425.8
3500.00	2.0	.37	20.0	10.6	12.5	157.4	7.4	175.0	376.2
4000.00	1.8	.39	19.2	10.0	11.1	135.7	7.4	144.5	348.8
4500.00	2.0	.45	18.6	9.3	10.4	118.2	7.3	108.0	302.3
5000.00	2.0	.37	18.1	8.8	9.5	103.7	7.3	81.8	266.4
5500.00	2.0	.44	17.7	8.3	8.8	91.0	7.4	64.8	241.8
6000.00	1.8	.64	16.3	7.3	9.3	80.4	7.2	55.9	217.6
6500.00	1.7	.66	15.6	6.7	9.2	72.2	7.2	44.7	193.6
7000.00	1.5	.90	14.5	6.1	9.6	65.3	6.9	38.5	172.1
7500.00	1.4	1.26	15.8		6.5	55.6		17.8	150.8
8000.00	1.3	1.19	15.5		5.6	50.5		13.0	140.2
8500.00	1.1	1.00	13.1	5.1	9.4	50.6	6.9	26.4	142.6
9000.00	1.1	1.23	15.6		.1	45.8		9.9	133.6
9500.00	1.1	1.65	14.1		5.4	42.0		12.9	126.0
10000.00	.9	.90	12.3	4.5	9.1	39.7	7.0	19.1	119.7
10500.00	.6	.71	11.9	4.1	9.4	36.4	7.1	15.8	110.0
11000.00	.4	.72	11.9	3.9	9.5	33.9	7.6	13.9	108.6
11500.00	.4	.36	12.7	3.9	9.2	31.3	8.4	9.3	96.4
12000.00	.4	.14	12.9	3.6	9.5	28.5	8.9	8.1	96.4
12500.00	.1	.17	12.7	3.3	9.9	26.3	9.3	6.5	89.3
13000.00	-.1	.08	13.3	3.1	10.4	23.8	10.3	4.7	84.1
13500.00	-.1	-.17	15.0	2.7	11.2	21.4	12.4	2.9	82.8
14000.00	-.2	-.44		2.4	12.3	19.0		-.1	71.9
14500.00	-1.7	.05	18.2	2.2	12.7	16.4	17.8	.4	56.0
15000.00	-7.6	3.82	-4.1		10.1	13.1		31.5	30.1
15500.00	1.6	.75	6.0	2.4	10.5	.6	2.0	68.7	88.0
16000.00	2.4	.57	8.2	1.7	14.1	-8.1	4.1	36.7	106.6

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F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.596	3.179	-.005	-.178	11.897	-1.942	1.906	.778,
3.00	.374	4.356	.001	-.260	11.275	-2.660	1.593	1.064,
4.00	.392	6.434	.037	-.338	11.477	-2.832	1.438	2.184,
5.00	.915	8.413	.077	-.398	11.382	-3.244	1.695	3.233,
6.00	1.503	10.252	.088	-.437	13.118	-5.085	1.972	4.169,
7.00	1.928	12.267	.181	-.477	13.133	-5.608	1.917	5.396,
8.00	2.897	14.698	.265	-.507	14.352	-7.115	2.178	6.652,
9.00	4.160	17.262	.322	-.502	15.538	-10.461	2.124	8.119,
10.00	5.484	19.883	.495	-.254	16.787	-9.736	2.053	9.788,
11.00	7.888	24.332	.784	-.206	20.199	-12.311	2.673	12.615,

F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX),
2.00	14.807	1.2479	15.310	0.000	11.0,
3.00	17.514	.6234	0.000	16.495	22.5,
4.00	23.936	.4130	0.000	15.414	62.9,
5.00	17.771	.6890	0.000	14.858	38.7,
6.00	14.233	1.1150	12.930	0.000	30.9,
7.00	15.640	1.0562	13.020	0.000	42.4,
8.00	13.821	1.3566	10.907	0.000	39.3,
9.00	13.335	1.6051	10.408	0.000	41.8,
10.00	14.787	1.5455	11.076	0.000	54.9,
11.00	13.969	1.5053	10.450	0.000	54.9,

Run
#46-3

F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.067	3.356	.001	-.128	16.042	-2.089	1.017	1.515,
3.00	.553	4.615	.011	-.177	15.794	-3.288	1.115	2.033,
4.00	.463	6.509	.036	-.206	15.319	-3.560	.981	2.972,
5.00	.859	8.611	.070	-.211	16.061	-3.784	1.122	4.178,
6.00	1.430	10.568	.104	-.167	17.082	-5.327	1.294	5.089,
7.00	1.854	12.982	.131	-.100	17.700	-6.254	1.321	6.092,
8.00	2.683	15.312	.196	.060	18.167	-7.734	1.317	6.926,
9.00	3.435	18.078	.296	.254	20.569	-9.341	1.285	7.986,
10.00	5.655	22.453	.439	.682	23.317	-10.144	1.886	9.858,
11.00	7.613	28.136	.572	1.220	26.667	-14.464	1.796	12.218,

	F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX),
	2.00	31.214	.1862	0.000	21.024	72.7,
	3.00	21.632	.5751	0.000	19.599	36.2,
EG	4.00	28.140	.3327	0.000	18.772	102.1,
EG	5.00	26.105	.4349	0.000	19.697	101.0,
	6.00	29.951	.8014	0.000	19.587	188.7,
	7.00	28.419	1.0319	19.460	0.000	184.5,
EG	8.00	34.590	.7485	0.000	19.830	429.1,
EG	9.00	18.764	.0419	0.000	17.631	78.1,
	10.00	25.721	.2027	0.000	14.964	193.2,
EG	11.00	21.631	-.1361	0.000	13.524	132.7,

Run
#46-8

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F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.101	3.347	-.001	-.170	10.850	-1.837	1.517	1.353,
3.00	.357	4.768	.012	-.253	10.562	-2.491	1.545	1.893,
4.00	.424	6.483	.033	-.316	10.490	-2.763	1.549	2.972,
5.00	.798	8.620	.093	-.336	11.074	-2.912	1.655	4.367,
6.00	1.283	10.664	.140	-.352	11.790	-4.100	1.837	5.492,
7.00	1.831	13.108	.162	-.299	12.051	-4.840	1.896	6.765,
8.00	2.557	15.567	.274	-.137	12.650	-5.656	1.987	7.940,
9.00	3.325	18.352	.414	-.037	14.205	-6.806	1.938	9.180,
10.00	5.314	22.554	.634	.224	15.720	-7.544	2.457	11.232,
11.00	7.570	27.272	.837	.357	17.530	-10.777	2.236	13.813,

F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX),
2.00	22.786	.3337	0.000	18.116	27.6,
3.00	18.398	.5837	0.000	16.324	24.9,
4.00	19.697	.5336	0.000	15.335	38.6,
5.00	20.357	.6495	0.000	15.166	52.1,
6.00	17.275	.9514	0.000	15.176	43.8,
7.00	14.271	1.4569	11.814	0.000	36.2,
8.00	14.517	1.7642	11.483	0.000	42.6,
9.00	20.211	1.1085	13.781	0.000	92.2,
10.00	13.672	1.2335	11.227	0.000	48.3,
11.00	16.480	.8197	0.000	13.545	73.4,

Run #46-26

F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	.062	2.973	.016	-.137	7.545	-1.536	.672	1.904,
3.00	.239	4.195	.037	-.207	7.265	-2.274	.757	2.642,
4.00	.333	5.762	.059	-.253	7.104	-2.642	.676	3.743,
5.00	.638	7.702	.127	-.265	7.403	-3.005	.772	5.098,
6.00	.999	9.421	.170	-.266	7.600	-3.914	.809	6.108,
7.00	1.251	11.362	.227	-.219	7.658	-4.496	.709	7.131,
8.00	1.843	13.335	.261	-.062	7.838	-5.239	.691	8.024,
9.00	2.372	15.785	.389	.064	8.680	-6.626	.387	9.028,
10.00	3.857	19.449	.547	.319	9.586	-7.230	.725	11.182,
11.00	5.585	24.354	.766	.718	11.337	-9.134	.302	13.519,

	F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX),
EG	2.00	22.751	.1643	0.000	17.466	27.5,
EG	3.00	21.969	.3510	0.000	15.591	37.6,
EG	4.00	18.574	.3562	0.000	14.647	33.9,
EG	5.00	15.264	.3571	0.000	14.349	29.0,
EG	6.00	15.457	.5041	0.000	14.320	35.6,
EG	7.00	13.361	.3661	0.000	14.498	32.6,
EG	8.00	14.341	.3255	0.000	15.452	41.7,
EG	9.00	10.624	-.4554	0.000	14.426	30.6,
EG	10.00	11.514	-.2571	0.000	12.778	37.6,
EG	11.00	8.730	-.7764	0.000	11.421	30.1,

Run #46-27

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F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO)	
2.00	.265	5.036	.008	-.196	12.397	-2.006	1.200	1.503
3.00	.448	6.891	.018	-.279	11.870	-2.417	1.078	1.780
4.00	.784	9.394	.047	-.387	11.902	-2.844	1.066	2.792
5.00	1.339	12.429	.105	-.378	12.687	-4.046	1.172	4.112
6.00	2.229	13.082	.095	-.247	11.316	-7.214	1.199	3.356
7.00	3.592	19.044	.223	-.345	14.760	-7.471	1.353	6.250
8.00	5.880	23.755	.330	-.216	16.261	-10.058	1.377	7.279
9.00	9.294	29.448	.498	-.085	17.961	-14.098	1.232	8.304
10.00	17.056	37.284	.839	.105	21.363	-20.650	1.414	10.506
11.00	30.470	38.413	1.210	.059	17.133	-31.146	1.543	11.080
12.00	60.908	24.886	1.577	-.488	-4.192	-48.704	7.621	15.579

F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX)
2.00	22.639	.3757	0.000	18.067	27.1
3.00	20.511	.5107	0.000	16.489	31.8
4.00	21.473	.5648	0.000	15.655	47.4
5.00	22.774	.6535	0.000	15.332	68.8
6.00	14.329	1.4028	11.940	0.000	31.2
7.00	16.210	1.3248	12.636	0.000	45.2
8.00	15.055	1.7260	11.898	0.000	45.3
9.00	16.321	1.3674	12.845	0.000	58.9
10.00	15.366	1.1197	13.355	0.000	58.7
11.00	10.672	1.6595	9.927	0.000	37.6
12.00	.976	$$$$$$	.964	0.000	13.4

Run
#48-21

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9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 50-1
BIAS= 3.50 VOLTS,

Run #50-1

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000.00	.10	3.07	14.36	-1.84	.01	-.27	1.34	1.59
2500.00	.22	3.79	14.61	-2.60	.02	-.33	1.41	1.88
3000.00	.43	4.70	14.94	-3.45	.02	-.40	1.52	2.32
3500.00	.60	5.46	15.28	-3.85	.03	-.45	1.62	2.69
4000.00	.64	6.52	15.84	-4.13	.06	-.50	1.64	3.24
4500.00	.76	7.77	16.47	-4.95	.09	-.56	1.71	3.95
5000.00	1.13	8.98	16.78	-6.27	.09	-.60	1.81	4.62
5500.00	1.07	10.20	17.22	-6.77	.14	-.63	1.75	5.26
6000.00	1.56	11.86	17.81	-7.31	.17	-.66	1.80	6.14
6500.00	2.10	13.28	18.06	-8.61	.19	-.68	1.98	6.98
7000.00	2.40	14.87	18.47	-9.67	.24	-.69	1.89	7.84
7500.00	2.92	16.31	19.16	-10.72	.29	-.70	2.04	8.61
8000.00	3.43	17.91	18.61	-11.53	.31	-.65	2.03	9.37
8500.00	3.87	19.62	18.84	-11.64	.34	-.60	2.06	10.20
9000.00	4.72	21.50	20.16	-12.52	.27	-.36	2.69	10.95
9500.00	5.77	23.00	20.69	-14.17	.52	-.26	2.74	11.33
10000.00	6.99	25.00	20.50	-16.03	.69	-.17	2.75	12.30
10500.00	8.37	25.94	19.69	-17.19	.82	-.23	2.94	12.50
11000.00	8.91	28.00	19.84	-18.69	.82	-.11	2.39	13.14
11500.00	10.39	29.09	19.09	-20.50	.89	-.01	2 54	13.80
12000.00	11.70	30.03	18.12	-22.12	.93	.09	2.25	13.94
12500.00	12.87	31.56	17.25	-23.50	1.00	.19	1.82	14.73
13000.00	15.50	33.31	15.94	-26.91	1.05	.24	1.39	15.34
13500.00	19.81	35.31	13.56	-31.50	1.05	.39	1.21	16.41
14000.00	24.64	36.31	10.86	-35.37	.82	.88	.24	18.28
14500.00	35.19	39.00	5.93	-34.06	2.65	5.55	6.53	26.53
15000.00	48.19	18.47	-11.59	-53.31	2.15	-4.30	3.84	13.20
15500.00	48.19	-.35	-36.50	-43.31	-1.29	-2.86	3.25	17.72
16000.00	34.12	-13.44	-45.19	-14.02	-2.97	.39	5.95	18.00

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 50-1
BIAS= 3.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	2.5	.15	24.6	15.9	12.5	307.4	6.2	272.7	352.0
2500.00	2.5	.25	21.6	13.1	16.1	247.7	6.0	222.7	318.4
3000.00	2.6	.39	18.5	10.3	20.6	199.0	5.6	174.4	275.4
3500.00	2.6	.46	17.1	9.2	20.7	170.7	5.3	146.7	248.0
4000.00	2.7	.38	17.1	9.1	15.4	143.6	5.3	111.3	223.0
4500.00	2.9	.41	16.4	8.4	13.4	120.7	5.1	85.4	193.4
5000.00	2.9	.57	14.8	7.1	14.6	104.3	4.9	70.6	170.7
5500.00	2.9	.46	15.4	7.5	11.0	92.2	5.0	55.9	156.4
6000.00	2.7	.56	14.1	6.4	11.4	79.1	5.0	44.4	137.9
6500.00	2.4	.75	12.7	5.6	12.1	70.3	4.7	38.9	123.0
7000.00	2.3	.73	12.7	5.4	10.9	62.9	5.0	30.6	112.7
7500.00	2.2	.82	12.1	5.0	10.9	57.0	4.8	27.5	103.3
8000.00	1.8	.97	11.5	4.8	10.5	52.0	4.9	23.7	96.7
8500.00	1.3	1.07	13.4		2.6	42.8		5.5	81.9
9000.00	1.1	2.30	10.8		7.7	41.3		15.8	79.9
9500.00	1.1	1.69	11.5		5.3	38.8		10.6	79.2
10000.00	.7	1.45	11.7		4.1	35.6		8.8	74.1
10500.00	.2	1.66	10.1		5.6	33.4		9.2	72.5
11000.00	.3	1.24	12.2		3.9	31.2		4.3	70.5
11500.00	-.0	1.45	11.0		4.7	29.8		6.2	67.8
12000.00	-.1	1.26	11.8		3.5	28.8		4.6	67.7
12500.00	-.4	.84	9.9	3.2	10.3	26.7	7.0	7.4	64.2
13000.00	-.3	.57	10.8	3.0	10.7	24.2	8.1	5.3	61.9
13500.00	-.5	.94	11.2	2.7	11.3	21.1	9.0	4.0	58.0
14000.00	-.6	-.64	1.8	2.4	12.1	16.7	.0	-.3	52.8
14500.00	-5.4	1.20	4.8		5.4	21.7		2.6	36.4
15000.00	.1	2.37	4.0		12.0	4.4		25.8	61.1
15500.00	1.2	2.20	6.4		15.4	-7.2		13.2	59.3
16000.00	1.3	1.38	6.6		31.6	-25.8		10.1	54.7

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F(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	-.193	3.513	.000	-.106	12.890	-2.153	.474	1.242,
3.00	.151	4.935	.001	-.153	12.422	-3.436	.644	1.651,
4.00	.074	6.768	.004	-.203	11.885	-3.824	.564	2.561,
5.00	.648	8.976	.038	-.211	12.649	-4.222	.798	3.674,
6.00	.974	11.613	.072	-.223	13.274	-4.945	.725	4.752,
7.00	1.496	14.448	.109	-.185	13.981	-5.764	.646	5.920,
8.00	3.037	17.436	.165	-.142	15.457	-7.465	.858	6.966,
9.00	4.290	19.422	.215	-.080	16.139	-9.966	1.495	8.186,
10.00	4.819	23.663	.275	.057	17.263	-12.082	.981	9.091,
11.00	4.656	27.630	.352	.349	19.480	-7.482	-.678	10.048,
12.00	18.898	27.806	.818	.392	15.053	-28.705	4.445	10.452,

	F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX),
EG	2.00	26.582	.0308	0.000	20.922	42.7,
	3.00	26.602	.3615	0.000	19.247	64.2,
EG	4.00	36.531	.3193	0.000	17.896	268.3,
	5.00	30.196	.5072	0.000	17.938	161.7,
EG	6.00	22.876	.4684	0.000	17.818	83.5,
EG	7.00	19.961	.4519	0.000	18.467	69.7,
	8.00	31.657	.9923	0.000	18.956	306.2,
	9.00	14.739	2.3394	12.697	0.000	49.1,
EG	10.00	37.490	.6790	0.000	18.753	749.1,
EG	11.00	10.280	$$$$$$	0.000	16.243	35.9,
	12.00	5.634	4.9090	5.654	0.000	23.0,

Run #50-5

(GHZ)	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	-.209	2.937	.008	-.093	12.339	-2.033	-.032	1.282,
3.00	.106	4.033	.008	-.138	11.801	-3.188	.140	1.572,
4.00	.053	5.509	.033	-.163	11.245	-3.369	-.003	2.495,
5.00	.512	7.348	.077	-.189	11.918	-3.716	.269	3.721,
6.00	.714	9.343	.127	-.220	12.526	-4.203	.207	4.842,
7.00	1.134	11.390	.159	-.234	13.091	-4.842	.058	6.056,
8.00	1.975	13.467	.210	-.200	14.300	-5.889	.467	7.293,
9.00	2.968	15.625	.243	-.091	15.337	-7.927	1.133	7.840,
0.00	3.395	18.617	.474	.024	17.563	-9.959	-.136	9.135,
1.00	2.286	22.122	.572	.220	17.367	-6.714	-1.487	10.548,
2.00	13.650	22.116	.929	.133	17.991	-20.132	4.008	11.635,

	F (GHZ)	U (DB)	K	MAG(DB)	MSG(DB)	F(MAX),
G	2.00	26.364	.0910	0.000	21.254	41.6,
G	3.00	26.443	.2191	0.000	19.480	63.0,
G	4.00	19.591	.0901	0.000	18.482	38.2,
G	5.00	16.922	.0260	0.000	17.860	35.1,
G	6.00	14.687	-.1102	0.000	17.165	32.5,
G	7.00	13.698	-.2050	0.000	16.929	33.9,
G	8.00	14.420	.0028	0.000	17.267	42.1,
G	9.00	23.006	.8315	0.000	18.231	127.2,
G	10.00	10.474	-.9903	0.000	16.292	33.4,
G	11.00	7.918	$$$$$$	0.000	14.826	27.4,
	12.00	6.644	3.5542	6.162	0.000	25.8,

Run #50-12

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FROM COPY FURNISHED TO DDC

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-1*
BIAS= 3.50 VOLTS,

Run #53-1

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000.00	.27	4.37	21.28	-2.84	.01	-.19	.92	1.49
2500.00	.52	5.49	21.59	-3.99	.02	-.23	.96	1.71
3000.00	.89	6.81	21.97	-5.31	.02	-.27	1.08	2.07
3500.00	1.12	7.99	22.62	-5.93	.04	-.29	1.18	2.35
4000.00	1.34	9.59	23.50	-6.63	.06	-.31	1.22	2.75
4500.00	1.73	11.42	24.50	-8.06	.09	-.32	1.30	3.31
5000.00	2.53	13.22	24.75	-10.47	.15	-.33	1.57	3.76
5500.00	2.69	15.27	25.19	-11.23	.17	-.40	1.37	3.87
6000.00	3.74	17.69	26.28	-12.45	.16	-.37	1.34	4.60
6500.00	5.16	19.78	26.59	-14.66	.15	-.26	1.62	5.14
7000.00	6.25	21.72	26.75	-16.69	.29	-.19	1.42	5.65
7500.00	7.53	24.03	28.19	-18.97	.39	-.14	1.62	6.23
8000.00	8.92	26.28	27.34	-20.75	.45	-.03	1.96	6.48
8500.00	10.66	29.06	27.87	-21.62	.63	.09	1.71	6.77
9000.00	13.48	31.97	29.66	-25.00	.79	.15	1.87	7.44
9500.00	16.53	34.12	29.91	-29.41	.88	.30	2.07	7.67
10000.00	22.19	35.50	27.53	-34.31	1.19	.45	1.96	8.31
10500.00	25.22	32.31	24.25	-37.37	1.40	.33	2.27	8.55
11000.00	27.37	35.00	22.00	-41.81	1.57	.45	1.72	8.58
11500.00	31.44	35.12	18.56	-46.19	1.74	.45	1.34	9.33
12000.00	36.75	32.87	12.22	-51.00	1.85	.37	.99	9.78
12500.00	40.69	29.22	3.62	-53.75	1.88	.31	.50	10.67
13000.00	44.81	20.78	-11.00	-52.75	1.87	.09	-.16	11.75
13500.00	43.94	11.56	-23.00	-44.00	1.39	.04	-.28	13.56
14000.00	38.62	5.20	-27.94	-32.81	.56	.93	-.03	15.52
14500.00	36.37	8.66	-24.00	-20.16	.95	5.01	5.31	19.47
15000.00	39.19	-13.11	-29.03	-25.56	7.02	-4.06	5.06	7.33
15500.00	22.37	-16.97	-34.75	-12.50	.81	-2.32	1.37	12.52
16000.00	13.72	-11.50	-27.03	-.07	.38	-.03	2.13	13.11

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-1*
BIAS= 3.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	5.9	.19	26.0	12.6	14.3	218.4	7.6	259.8	447.7
2500.00	5.8	.29	23.1	10.0	17.1	172.9	7.3	216.0	400.0
3000.00	5.7	.46	20.5	8.1	18.5	138.5	6.7	176.8	340.2
3500.00	5.7	.51	19.5	7.3	16.9	118.0	6.4	153.7	305.1
4000.00	5.7	.48	19.0	7.0	13.8	98.5	6.3	122.9	272.3
4500.00	5.7	.55	18.1	6.3	12.6	82.6	6.0	96.9	237.5
5000.00	5.4	.79	16.1	5.3	13.4	70.6	5.4	88.5	206.6
5500.00	5.3	.62	16.4	5.4	10.8	61.4	5.8	78.4	206.2
6000.00	5.0	.90	15.5	4.6	11.2	52.5	5.9	59.6	184.4
6500.00	4.6	1.78	15.0		8.1	42.9		36.0	158.4
7000.00	4.4	1.19	16.9		3.7	39.2		11.6	154.1
7500.00	4.3	1.12	17.0		2.8	36.2		8.9	142.8
8000.00	3.7	1.49	14.7		5.4	33.8		19.8	138.9
8500.00	3.3	.74	13.1	3.5	10.1	30.2	6.2	28.0	131.6
9000.00	3.2	.71	12.6	3.3	10.1	26.6	6.0	24.4	118.7
9500.00	3.1	.66	12.0	3.1	10.4	23.8	5.8	24.3	113.9
10000.00	2.6	.69	11.6	2.7	11.3	20.5	6.3	18.3	104.7
10500.00	2.5	1.06	13.4		2.8	23.4		.7	106.2
11000.00	2.6	.51	11.6	2.3	12.3	17.9	6.6	15.4	98.9
11500.00	2.6	.35	12.2	2.2	12.5	15.9	7.4	10.9	91.7
12000.00	2.5	.31	12.5	1.9	13.5	13.6	8.1	8.7	87.8
12500.00	2.5	.16	13.7	1.7	14.6	11.7	9.5	5.5	81.9
13000.00	2.3	.01	15.2	1.3	16.7	8.5	11.6	3.0	76.3
13500.00	1.8	.09	16.1	.9	20.0	5.6	13.5	1.7	69.3
14000.00	1.2	-.38	1.7	.5	24.7	4.4	.0	-.9	61.4
14500.00	-3.5	1.91	2.4		22.7	20.0		7.9	45.5
15000.00	-1.8	2.24	.5		15.9	-1.8		61.5	62.2
15500.00	2.0	1.31	8.4		10.8	-16.5		14.5	89.3
16000.00	1.3	6.74	7.3		40.9	-29.9		14.0	73.7

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

F(GHZ	Y11(MMHO)		Y12(MMHO)		Y21(MMHO)		Y22(MMHO),	
2.00	-.189	4.711	.005	-.176	19.981	-3.234	.080	1.808,
3.00	.351	6.429	.021	-.263	21.070	-4.896	-.209	1.627,
4.00	.217	8.865	.051	-.311	21.026	-6.118	.234	2.535,
5.00	1.094	11.944	.095	-.373	23.283	-8.581	.296	3.136,
6.00	2.210	16.127	.172	-.396	25.726	-13.499	.596	4.687,
7.00	4.620	19.170	.206	-.432	26.726	-21.770	.940	5.095,
8.00	3.818	19.510	.239	-.095	19.334	-16.854	.229	5.538,
9.00	8.210	25.803	.429	-.010	20.621	-21.401	.497	7.251,
10.00	12.590	28.167	.701	.129	22.061	-31.711	.461	7.335,
11.00	17.872	28.974	1.117	.117	12.984	-41.685	.816	7.612,
12.00	22.311	32.816	1.075	.158	1.549	-32.724	.529	11.821,

	F (GHZ)	U (DB)	K	MAG (DB)	MSG (DB)	F(MAX),
EG	2.00	29.410	.1226	0.000	20.612	59.09,
EG	3.00	23.473	.1212	0.000	19.139	44.75,
EG	4.00	20.660	.1357	0.000	18.420	43.16,
EG	5.00	19.053	.1719	0.000	18.098	44.83,
EG	6.00	18.231	.2842	0.000	18.231	48.95,
EG	7.00	23.982	.7632	0.000	18.577	$$$$$,
EG	8.00	16.348	-.1917	0.000	19.991	52.54,
EG	9.00	16.565	-.0368	0.000	18.404	60.60,
EG	10.00	15.804	-.2880	0.000	17.339	51.69,
	11.00	37.282	.1998	0.000	15.897	$$$$$,
	12.00	14.265	.4709	0.000	14.795	62.00,

Run
#53-9

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-10
BIAS= 3.50 VOLTS,

Run #53-10

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000.00	.21	4.06	20.19	-2.72	.01	-.22	1.11	1.37
2500.00	.42	5.11	20.59	-3.82	.02	-.27	1.17	1.61
3000.00	.75	6.29	20.87	-5.05	.02	-.31	1.30	1.97
3500.00	.93	7.33	21.50	-5.65	.04	-.35	1.40	2.25
4000.00	1.09	8.78	22.34	-6.20	.06	-.38	1.43	2.69
4500.00	1.40	10.37	23.22	-7.48	.09	-.42	1.48	3.26
5000.00	2.05	12.03	23.59	-9.44	.09	-.44	1.57	3.82
5500.00	2.16	13.67	24.44	-10.44	.14	-.44	1.50	4.35
6000.00	2.99	15.75	25.28	-11.56	.18	-.44	1.57	5.10
6500.00	3.88	17.62	25.66	-13.50	.21	-.43	1.81	5.76
7000.00	4.79	19.56	25.87	-15.55	.27	-.40	1.68	6.47
7500.00	5.67	21.44	26.78	-17.31	.34	-.36	1.83	7.10
8000.00	6.57	23.41	26.19	-18.59	.38	-.30	1.85	7.75
8500.00	7.84	25.56	26.50	-19.12	.44	-.14	1.89	8.31
9000.00	9.66	28.09	28.22	-21.62	.56	-.04	2.09	9.17
9500.00	11.69	29.81	28.47	-24.91	.69	.09	2 44	9.67
10000.00	14.69	31.62	27.03	-28.47	.79	.22	2.59	10.52
10500.00	16.28	31.37	24.62	-29.53	.99	.35	2.69	10.53
11000.00	18.19	34.87	24.91	-32.25	1.16	.50	2.04	11.09
11500.00	21.91	35.50	24.97	-36.44	1.34	.57	1.99	12.06
12000.00	25.09	39.37	21.91	-41.62	1.49	.62	1.95	12.41
12500.00	27.59	35.19	17.06	-44.37	1.57	.59	1.50	13.17
13000.00	33.31	34.12	9.56	-49.87	1.64	.54	.91	13.84
13500.00	39.31	29.31	-2.20	-52.12	1.45	.48	.52	15.23
14000.00	43.06	23.78	-11.17	-50.87	.86	1.01	-.21	17.34
14500.00	44.91	19.59	-23.97	-39.12	.06	4.41	3.58	23.56
15000.00	46.12	-12.31	-39.19	-45.44	5.43	-6.80	2.71	7.21
15500.00	31.37	-13.80	-43.69	-21.91	.04	-2.62	1.71	15.52
16000.00	21.97	-12.98	-37.62	-4.54	-.98	-.14	3.15	16.31

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-10
BIAS= 3.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	5.4	.18	25.8	13.5	12.9	233.6	6.8	303.9	408.6
2500.00	5.4	.32	22.6	10.7	16.5	189.2	6.5	251.2	366.8
3000.00	5.3	.47	19.9	8.5	18.8	149.2	6.1	202.0	316.0
3500.00	5.3	.49	18.9	7.8	17.2	128.1	5.8	174.0	284.4
4000.00	5.4	.45	18.6	7.5	13.9	107.2	5.7	136.1	256.2
4500.00	5.4	.51	17.7	6.8	12.7	90.4	5.5	106.2	225.4
5000.00	5.2	.72	16.1	5.6	13.7	77.5	5.3	88.5	200.4
5500.00	5.3	.82	16.4	5.8	11.2	68.6	5.4	69.9	185.4
6000.00	5.0	.74	15.4	5.1	11.3	59.1	5.3	55.4	163.7
6500.00	4.6	1.03	16.6		.9	46.5		13.0	131.2
7000.00	4.4	1.01	17.4		2.0	41.9		-.0	125.0
7500.00	4.3	1.11	18.1		4.1	38.6		9.7	117.2
8000.00	3.8	1.29	15.0		5.0	35.8		11.5	111.5
8500.00	3.3	1.36	14.9		4.0	34.2		11.7	108.8
9000.00	3.2	1.29	15.0		3.4	31.6		9.0	100.8
9500.00	3.0	1.31	14.0		4.4	30.0		6.9	97.0
10000.00	2.5	1.50	12.6		5.5	27.6		9.6	89.5
10500.00	2.1	1.51	12.3		4.7	27.5		8.5	89.0
11000.00	2.1	.54	11.6	3.0	10.4	22.5	6.5	11.6	81.4
11500.00	2.1	.51	11.7	2.7	11.1	20.4	6.9	9.3	74.8
12000.00	2.2	.50	11.6	2.5	11.8	18.8	7.0	8.7	72.0
12500.00	1.9	.34	12.1	2.3	12.3	17.5	7.9	6.4	68.5
13000.00	1.8	.21	13.1	2.0	13.2	14.8	9.3	4.3	65.4
13500.00	1.5	.24	13.9	1.4	15.1	12.1	10.8	2.7	60.9
14000.00	1.3	-.86	2.6	1.3	16.9	10.3	.0	-1.5	54.7
14500.00	-1.6	.71	9.1	1.2	17.5	9.9	9.7	2.3	38.6
15000.00	1.1	1.46	4.3		9.3	-1.4		71.0	80.5
15500.00	2.6	1.30	9.4		9.7	-14.8		9.1	72.0
16000.00	2.0	2.68	8.7		34.3	-33.3		8.1	61.1

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-11
BIAS= 3.50 VOLTS,

Run #53-11

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000.00	.23	4.27	21.72	-3.00	.01	-.20	1.00	1.33
2500.00	.48	5.36	22.22	-4.29	.02	-.24	1.09	1.55
3000.00	.81	6.61	22.59	-5.65	.02	-.29	1.21	1.90
3500.00	1.08	7.73	23.16	-6.34	.04	-.32	1.32	2.15
4000.00	1.25	9.25	24.09	-6.83	.07	-.35	1.32	2.61
4500.00	1.59	10.98	25.22	-8.37	.09	-.37	1.41	3.17
5000.00	2.31	12.72	25.56	-10.59	.11	-.39	1.50	3.73
5500.00	2.48	14.53	26.44	-11.75	.15	-.38	1.45	4.23
6000.00	3.41	16.78	27.44	-13.12	.19	-.37	1.54	5.00
6500.00	4.39	18.69	27.81	-15.28	.22	-.37	1.77	5.70
7000.00	5.52	20.78	28.00	-17.66	.26	-.30	1.77	6.35
7500.00	6.70	22.47	28.75	-19.37	.35	-.24	1.88	6.98
8000.00	7.41	24.66	28.87	-21.28	.24	-.12	2.15	7.64
8500.00	8.78	26.97	28.81	-21.94	.55	.10	2.02	8.08
9000.00	10.81	29.53	30.59	-24.44	.71	.20	2.21	8.98
9500.00	12.95	31.19	30.87	-28.34	.85	.32	2.60	9.37
10000.00	16.06	32.94	29.06	-32.37	1.05	.46	2.49	10.14
10500.00	18.44	32.75	26.53	-34.31	1.24	.51	2.66	10.67
11000.00	20.22	35.19	25.41	-37.69	1.40	.66	2.30	11.03
11500.00	22.91	35.69	23.12	-40.94	1.55	.73	2.16	11.80
12000.00	25.91	35.81	20.25	-44.06	1.66	.82	1.87	12.19
12500.00	28.59	35.62	16.28	-46.56	1.78	.89	1.45	13.08
13000.00	34.75	34.94	8.87	-52.37	1.95	.99	.89	13.92
13500.00	41.37	29.78	-3.46	-54.87	2.05	1.19	.63	15.44
14000.00	45.19	23.03	-13.42	-50.12	2.31	2.84	1.03	18.78
14500.00	47.50	5.23	-25.44	-54.50	4.41	-3.89	3.26	10.41
15000.00	39.56	-4.39	-39.37	-37.19	.91	-2.17	.70	15.05
15500.00	29.69	-9.16	-43.31	-19.47	-.38	-.75	1.80	17.56
16000.00	21.34	-7.84	-35.75	-3.86	-1.19	1.52	3.09	17.81

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10 DECEMBER 1975

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FET TESTS, COMMON SOURCE
SER# 53-11
BIAS= 3.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	6.1	.19	26.4	13.2	12.9	223.0	7.2	304.3	439.1
2500.00	6.1	.30	23.2	10.3	16.6	176.8	6.8	257.0	391.8
3000.00	6.0	.47	20.6	8.3	18.4	142.4	6.3	205.9	332.4
3500.00	5.9	.50	19.4	7.4	17.4	121.3	6.0	179.9	299.6
4000.00	6.0	.45	19.1	7.1	13.9	101.6	5.9	136.9	269.5
4500.00	6.0	.51	18.2	6.5	12.6	85.5	5.7	108.2	234.0
5000.00	5.8	.74	16.6	5.4	13.6	73.2	5.4	89.4	207.0
5500.00	5.8	.65	16.9	5.5	11.2	64.6	5.6	70.8	191.8
6000.00	5.5	.79	15.8	4.8	11.3	55.4	5.5	56.2	167.6
6500.00	5.1	1.11	16.7		3.8	44.0		14.3	136.5
7000.00	4.9	1.33	15.8		5.2	40.2		20.0	130.1
7500.00	4.7	1.34	15.6		5.5	37.5		16.5	122.9
8000.00	4.4	2.78	13.9		7.8	35.8		24.7	116.6
8500.00	3.9	.85	13.4	3.8	9.9	33.3	5.7	24.0	111.7
9000.00	3.7	.75	13.0	3.6	9.8	29.7	5.7	20.3	100.2
9500.00	3.6	.83	12.2	3.4	10.0	27.3	5.2	20.8	94.1
10000.00	3.2	.69	11.9	3.1	10.5	24.6	5.6	16.5	87.1
10500.00	2.7	.81	10.9	2.7	11.5	23.2	5.4	15.9	82.1
11000.00	2.7	.45	11.8	2.9	10.6	21.4	6.2	12.2	79.6
11500.00	2.4	.41	11.7	2.7	11.0	19.8	6.6	10.0	74.6
12000.00	2.3	.30	12.1	2.5	11.5	18.3	7.3	8.0	72.2
12500.00	2.1	.11	13.0	2.4	11.9	17.0	8.6	5.3	67.8
13000.00	2.0	-.07	14.6	2.1	12.5	14.4	10.5	3.1	63.6
13500.00	1.6	-.06	15.2	1.8	14.1	11.7	11.9	2.0	57.7
14000.00	.2	-.11	16.5	1.5	15.4	10.0	16.8	.5	46.8
14500.00	1.3	1.79	4.9		11.2	3.7		32.3	69.2
15000.00	2.6	1.35	10.1		9.7	-4.9		6.8	68.9
15500.00	2.7	2.66	10.5		23.7	-17.8		5.7	58.7
16000.00	1.5	1.19	10.1		137.1	5.5		3.2	52.4

9548WATS
10 DECEMBER 1975

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-12
BIAS= 3.50 VOLTS,

Run #53-12

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000.00	.28	4.41	20.87	-2.88	.01	-.21	.95	1.39
2500.00	.49	5.55	21.34	-4.03	.01	-.26	1.01	1.63
3000.00	.85	6.83	21.62	-5.37	.01	-.31	1.12	2.00
3500.00	1.12	7.98	22.25	-6.12	.03	-.34	1.21	2.29
4000.00	1.30	9.50	23.03	-6.72	.06	-.37	1.22	2.66
4500.00	1.59	11.27	23.97	-8.05	.08	-.40	1.25	3.21
5000.00	2.42	13.05	24.47	-10.09	.10	-.42	1.33	3.74
5500.00	2.57	14.89	25.44	-11.41	.14	-.42	1.26	4.22
6000.00	3.66	17.06	26.37	-12.87	.18	-.42	1.34	4.95
6500.00	4.72	19.09	26.72	-14.95	.21	-.41	1.54	5.63
7000.00	5.87	21.25	27.25	-17.31	.26	-.38	1.48	6.31
7500.00	7.26	23.31	28.50	-19.84	.33	-.34	1.62	6.92
8000.00	8.58	25.91	28.19	-22.16	.20	-.24	1.89	7.63
8500.00	10.39	27.91	27.91	-22.69	.54	-.04	1.73	7.84
9000.00	13.34	31.19	30.31	-26.62	.70	.03	1.90	8.64
9500.00	16.56	32.87	30.28	-31.69	.86	.10	2.16	8.91
10000.00	21.03	34.19	27.44	-37.19	1.04	.15	2.06	9.56
10500.00	23.53	34.00	24.09	-39.06	1.17	.18	1.96	9.92
11000.00	28.22	36.94	22.28	-44.81	1.39	.27	1.52	10.37
11500.00	33.37	36.44	18.06	-50.37	1.55	.23	1.41	11.33
12000.00	39.44	35.06	11.91	-55.75	1.64	.19	1.16	11.83
12500.00	44.87	31.31	3.17	-59.12	1.66	.07	.77	12.87
13000.00	51.50	21.75	-13.77	-60.56	1.45	-.13	.32	14.06
13500.00	52.44	6.27	-31.22	-51.69	.83	.03	.40	15.87
14000.00	45.44	-2.55	-39.94	-36.62	.09	1.48	.79	18.41
14500.00	38.50	3.64	-33.31	-9.11	7.33	4.40	11.66	17.53
15000.00	27.91	-22.75	-40.50	-18.87	.84	-1.87	2.89	14.03
15500.00	14.75	-14.25	-35.87	-1.80	.79	.22	4.14	15.52
16000.00	12.20	-7.97	-25.16	5.03	.65	.57	3.73	14.39

9548WATS
10 DECEMBER 1975.

VARIAN ASSOCIATES TEST REPORT
FET TESTS, COMMON SOURCE
SER# 53-12
BIAS= 3.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	5.7	.19	25.5	12.4	14.5	215.2	7.4	282.0	449.2
2500.00	5.7	.30	23.0	10.2	15.8	170.3	7.0	232.4	394.1
3000.00	5.6	.48	20.2	8.1	18.1	137.5	6.5	187.5	333.6
3500.00	5.6	.51	19.1	7.3	17.1	117.6	6.2	164.8	303.9
4000.00	5.6	.47	18.7	6.9	14.0	98.8	6.2	129.3	273.0
4500.00	5.6	.52	17.9	6.3	12.8	83.3	6.0	99.9	239.8
5000.00	5.4	.71	16.4	5.2	13.7	71.3	5.7	83.8	212.1
5500.00	5.4	.64	16.6	5.3	11.5	62.7	5.9	66.2	196.3
6000.00	5.1	.79	15.5	4.6	11.7	54.2	5.8	52.8	172.1
6500.00	4.8	1.07	16.5		4.5	41.8		5.0	139.6
7000.00	4.6	1.12	16.4		1.9	37.8		13.6	130.9
7500.00	4.5	1.25	15.6		4.2	34.7		11.2	123.0
8000.00	4.0	2.85	13.1		8.9	32.2		25.6	115.4
8500.00	3.5	1.10	16.3		2.1	31.3		7.0	117.8
9000.00	3.5	1.01	16.9		.6	28.0		4.1	107.6
9500.00	3.4	1.11	15.0		3.1	25.6		3.4	103.7
10000.00	3.1	1.07	14.8		1.7	23.2		5.5	96.2
10500.00	2.7	1.04	14.6		2.2	22.3		2.6	92.7
11000.00	2.6	.58	12.0	2.4	11.8	17.0	7.0	11.1	85.1
11500.00	2.5	.65	11.7	2.2	12.3	14.8	7.0	9.7	78.3
12000.00	2.4	.66	11.8	2.0	12.9	12.5	7.4	8.3	75.1
12500.00	2.2	.60	12.2	1.8	13.8	10.3	8.2	6.1	70.1
13000.00	2.2	.66	12.8	1.5	15.4	6.8	9.1	4.5	66.0
13500.00	1.9	1.31	15.3		8.0	9.2		2.5	61.4
14000.00	1.5	.27	2.2	.7	21.9	.2	.0	-.0	51.8
14500.00	-4.8	3.73	-2.6		20.3	5.7		22.8	33.7
15000.00	1.6	2.50	6.6		15.0	-13.6		20.8	71.3
15500.00	2.3	5.09	6.4		36.4	-26.9		18.1	57.4
16000.00	.7	4.98	4.8		57.6	-25.8		18.6	61.9

1001 2WATS
18 JUNE 1976

VARIAN ASSOCIATES TEST REPORT
FET 54

SER# 5
BIAS= ~~3.00~~ 2.95 VOLTS, Run #54-5

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000.00	.23	3.29	12.05	-1.69	.00	-.21	.81	1.14
2500.00	.37	4.03	12.86	-3.00	-.02	-.25	.82	1.45
3000.00	.54	4.93	12.09	-3.25	-.02	-.28	1.01	1.81
3500.00	.76	5.89	11.17	-4.16	.03	-.33	1.02	2.09
4000.00	.95	6.85	12.28	-2.45	.03	-.32	1.02	2.47
4500.00	1.19	7.84	14.66	-3.97	.04	-.44	.93	2.91
5000.00	1.35	9.08	14.22	-5.59	.03	-.47	1.14	3.57
5500.00	1.60	10.44	13.44	-7.29	.07	-.38	1.17	4.12
6000.00	2.12	11.80	13.27	-7.06	.12	-.39	1.12	4.66
6500.00	2.61	13.25	13.06	-7.69	.22	-.36	1.19	5.52
7000.00	3.15	14.52	19.19	-10.48	.26	-.45	1.11	6.09
7500.00	4.07	15.94	14.52	-12.06	.27	-.34	1.35	6.98
8000.00	4.65	17.09	13.56	-12.22	.29	-.33	1.44	7.45
8500.00	5.28	18.37	14.64	-11.56	.38	-.26	1.28	8.17
9000.00	6.14	19.78	14.92	-11.80	.45	-.16	1.40	8.93
9500.00	7.20	21.28	17.25	-11.86	.36	-.04	1.69	9.28
10000.00	8.45	22.81	14.39	-14.06	.64	.16	1.58	9.50
10500.00	10.05	24.12	17.06	-16.97	.93	.32	1.44	10.23
11000.00	11.34	25.94	16.97	-19.19	1.02	.39	1.89	10.98
11500.00	13.45	27.69	16.66	-21.47	1.12	.37	1.66	11.45
12000.00	16.03	29.28	15.81	-22.62	1.20	.56	1.24	12.42

1001 2WATS
18 JUNE 1976

VARIAN ASSOCIATES TEST REPORT
FET 54

SER# 5
BIAS= 3.00 VOLTS, 45.00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	1.1	.31	22.4	13.2	22.3	295.3	8.1	369.1	548.4
2500.00	1.7	.49	20.5	11.0	24.2	236.3	7.8	268.7	474.2
3000.00	1.0	.62	17.9	9.8	22.8	194.5	7.1	218.7	391.8
3500.00	.4	.63	16.0	8.6	21.9	162.1	7.0	182.0	361.3
4000.00	.6	.57	15.7	8.0	19.6	139.6	7.1	134.4	323.8
4500.00	2.0	.48	16.3	7.1	18.8	119.9	7.2	96.1	283.6
5000.00	1.7	.73	14.7	6.6	16.7	104.1	6.4	82.5	233.6
5500.00	1.4	.94	14.1	6.3	14.8	91.1	6.5	65.5	212.1
6000.00	.8	.97	13.0	5.5	14.9	80.3	6.7	50.8	192.8
6500.00	.4	.97	12.2	5.1	14.1	71.1	6.7	38.0	165.6
7000.00	3.2	.58	14.6	4.7	13.9	63.7	6.8	30.2	149.0
7500.00	1.2	1.38	12.7		7.0	51.7		16.1	123.2
8000.00	.9	1.65	11.5		8.5	46.7		15.9	118.6
8500.00	.3	1.28	12.9		5.5	45.7		4.6	111.5
9000.00	.0	1.38	12.4		6.0	43.7		5.0	109.2
9500.00	.2	2.46	10.9		9.3	42.0		11.2	102.7
10000.00	-.6	1.13	12.6		2.8	39.7		5.5	100.6
10500.00	.4	.33	11.1	2.9	13.3	35.1	7.8	10.1	91.6
11000.00	.2	.65	9.8	2.9	12.8	32.2	6.7	11.8	84.5
11500.00	.1	.55	10.1	2.7	12.9	29.0	7.2	9.6	81.2
12000.00	-.3	.22	11.2	2.5	13.1	26.2	9.1	5.5	75.8

/012WATS
/8 JUNE 1976

VARIAN ASSOCIATES TEST REPORT
FET 54

SER# 6
BIAS= .00 VOLTS, .00 MA

Run #54-6

Y REAL AND IMAGINARY:

FREQ	i1		21		i2		22	
2000.00	.13	3.43	9.36	-1.06	.01	-.17	.93	1.22
2500.00	.30	4.23	10.44	-2.54	.01	-.20	.70	1.71
3000.00	.50	5.10	9.64	-2.65	.01	-.23	.59	1.94
3500.00	.72	5.96	9.28	-3.70	.04	-.27	.83	2.39
4000.00	.74	6.93	10.28	-1.47	.06	-.26	.76	2.74
4500.00	.92	7.99	11.75	-3.37	.07	-.35	.92	3.15
5000.00	1.04	9.12	12.05	-4.91	.08	-.40	.87	3.59
5500.00	1.31	10.31	10.70	-5.54	.11	-.34	.97	4.23
6000.00	1.60	11.50	10.59	-5.46	.14	-.35	1.03	4.73
6500.00	2.05	12.70	9.59	-4.53	.22	-.33	.95	5.30
7000.00	2.23	13.91	12.80	-7.35	.25	-.45	1.01	6.10
7500.00	2.77	15.23	11.11	-9.02	.25	-.31	.99	6.62
8000.00	3.16	16.47	10.72	-8.41	.26	-.41	1.37	7.26
8500.00	3.77	17.69	11.67	-8.30	.33	-.33	1.08	7.73
9000.00	4.30	18.91	11.66	-8.30	.41	-.27	1.29	8.12
9500.00	4.97	20.22	13.61	-8.92	.39	-.25	1.39	8.67
10000.00	5.69	22.00	11.50	-10.02	.50	-.16	1.27	8.98
10500.00	6.78	23.34	13.73	-11.73	.68	-.03	1.44	9.61
11000.00	7.52	24.87	13.14	-12.69	.72	.08	1.36	10.19
11500.00	8.59	26.50	13.66	-13.97	.81	.04	1.46	11.22
12000.00	9.77	27.75	11.92	-13.98	.83	-.5	1.31	11.75

/012WATS
/8 JUNE 1976

VARIAN ASSOCIATES TEST REPORT
FET 54

SER# 6
BIAS= .00 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	-.9	.11	25.0	18.1	10.3	284.8	9.9	273.8	696.2
2500.00	-.0	.39	20.8	12.2	17.3	230.1	8.6	194.7	474.2
3000.00	-.8	.49	18.8	9.3	19.2	190.2	9.3	138.9	447.7
3500.00	-1.1	.67	15.8	8.9	19.9	161.5	7.9	130.7	360.2
4000.00	-.9	.32	16.6	9.1	14.7	140.2	8.4	89.8	324.2
4500.00	.2	.44	16.0	8.2	14.0	120.5	7.5	82.7	275.8
5000.00	.5	.51	15.9	7.8	12.5	105.3	7.6	65.1	247.7
5500.00	-.5	.79	13.9	7.1	12.3	93.7	7.3	53.0	215.6
6000.00	-.9	.83	12.8	6.6	12.0	83.8	7.1	45.1	194.3
6500.00	-2.3	.76	11.4	6.0	12.1	75.6	7.7	32.8	177.5
7000.00	.2	.59	13.2	5.8	11.2	68.5	7.2	27.8	152.3
7500.00	-.5	.95	12.2	5.3	11.5	62.5	7.5	23.3	143.6
8000.00	-1.5	1.42	10.6		6.5	52.1		15.4	118.4
8500.00	-1.4	1.02	14.0		.1	48.3		8.9	115.6
9000.00	-1.8	1.23	11.7		.0	46.3		10.0	111.9
9500.00	-1.3	1.39	11.7		4.3	43.5		7.2	106.1
10000.00	-2.2	1.25	11.6		3.7	40.1		3.8	104.1
10500.00	-1.3	.83	9.5	3.9	10.7	39.0	7.0	13.8	98.4
11000.00	-1.6	.72	9.6	3.8	10.4	36.4	7.4	11.4	93.3
11500.00	-1.7	.81	9.1	3.6	10.4	33.7	7.2	10.4	84.8
12000.00	-2.6	.79	8.7	3.4	10.6	31.7	7.9	8.2	81.7

Run
#56-2

PAGE 2: ANA*A5209/DEPT 0810 SEPTEMBER 26,1977
VARIAN METROLOGY LAB/LIONEL WINDHAM
INGAAS DEVICE

.00 VOLTS, .00 MA (MEAS 1) 56-2 4V

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	3.616	86	15.685	-7	.196	-87	1.643	68
2500.000	4.463	85	15.723	-9	.239	-87	1.921	69
3000.000	5.533	84	16.079	-11	.284	-86	2.302	73
3500.000	6.489	85	16.268	-11	.320	-84	2.746	76
4000.000	7.682	83	16.693	-12	.355	-83	3.224	78
4500.000	8.597	82	16.995	-16	.374	-82	3.451	77
5000.000	9.772	80	17.594	-17	.409	-78	3.954	76
5500.000	10.868	80	18.139	-18	.455	-79	4.392	77
6000.000	12.308	80	18.889	-19	.464	-78	4.946	79
6500.000	13.670	79	19.230	-20	.473	-75	5.471	80
7000.000	14.992	78	19.636	-22	.469	-75	5.979	81
7500.000	16.377	76	20.512	-23	.451	-72	6.458	81
8000.000	17.896	75	20.528	-26	.429	-69	6.925	81
8500.000	19.491	74	21.348	-25	.430	-72	7.336	82
9000.000	21.331	70	21.931	-29	.212	-87	7.838	81
9500.000	22.271	66	22.590	-29	.068	80	8.172	80
10000.00	22.292	66	23.705	-29	.320	37	8.717	82
10500.00	23.569	66	25.393	-34	.477	31	9.255	81
11000.00	25.488	65	25.643	-33	.500	33	9.864	81
11500.00	27.179	64	27.714	-38	.606	47	10.534	81
12000.00	29.175	62	29.005	-40	.799	54	11.144	80
12500.00	31.184	60	29.071	-41	.931	61	11.602	80
13000.00	33.313	58	33.035	-45	1.190	69	12.056	82
13500.00	35.448	55	31.479	-48	1.589	83	13.317	84
14000.00	39.617	49	31.590	-56	3.170	87	16.310	79

REF PLANE EXT(CM): IN= .00, OUT= .00

PAGE 3: ANA*A5209/DEPT 0810 SEPTEMBER 26,1977
VARIAN METROLOGY LAB/LIONEL WINDHAM
INGAAS DEVICE

.00 VOLTS, .00 MA (MEAS 1) 56-2 4V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000			3.37	-34.71	.17	4.34
2500.000			3.21	-33.14	.25	2.78
3000.000			3.22	-31.85	.27	2.32
3500.000			3.16	-30.98	.24	2.33
4000.000			3.08	-30.37	.29	1.70
4500.000			2.93	-30.21	.44	1.11
5000.000		16.34	2.83	-29.85	.50	.79
5500.000		15.42	2.75	-29.27	.59	.67
6000.000		15.23	2.74	-29.46	.60	.62
6500.000		14.71	2.51	-29.68	.64	.54
7000.000		14.06	2.28	-30.17	.77	.44
7500.000		13.31	2.18	-30.97	.97	.33
8000.000	13.94	12.51	1.72	-31.88	1.22	.26
8500.000	13.22	12.13	1.57	-32.35	1.40	.22
9000.000	10.88	10.85	1.15	-39.15	4.29	.07
9500.000	10.16	10.12	.94	-49.43	15.94	.02
10000.00	13.17	11.90	1.39	-36.02	1.93	.13
10500.00	14.75	11.95	1.60	-32.92	1.17	.18
11000.00	12.78	11.03	1.11	-33.08	1.54	.15
11500.00	13.00	11.15	1.28	-31.93	1.36	.17
12000.00	12.48	10.61	1.08	-30.12	1.27	.18
12500.00	11.62	10.11	.59	-29.30	1.31	.19
13000.00		12.27	1.28	-27.58	.68	.35
13500.00		14.22	.33	-25.61	.39	.78
14000.00		9.02	-1.28	-21.25	.74	.43

REF PLANE EXT(CM): IN= .00, OUT= .00

Run
#57-1

PAGE 2: ANA*A5209/DEPT 0810 SEPTEMBER 26,1977
VARIAN METROLOGY LAB/LIONEL WINDHAM
INGAAS DEVICE

.00 VOLTS, .00 MA (MEAS 1) *57-1

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	3.123	85	12.604	-7	.252	-89	1.593	66
2500.000	3.846	84	12.658	-10	.309	-88	1.825	66
3000.000	4.782	84	12.882	-11	.372	-88	2.204	71
3500.000	5.673	84	13.186	-12	.424	-86	2.658	75
4000.000	6.667	83	13.505	-13	.478	-84	3.108	77
4500.000	7.386	82	13.567	-17	.526	-85	3.312	76
5000.000	8.505	80	14.244	-18	.578	-84	3.801	76
5500.000	9.503	79	14.752	-19	.620	-83	4.254	77
6000.000	10.795	79	15.477	-20	.669	-81	4.842	79
6500.000	12.149	78	15.947	-22	.719	-80	5.462	80
7000.000	13.289	77	16.191	-24	.618	-89	6.064	79
7500.000	14.481	76	17.031	-24	.618	-73	6.425	78
8000.000	15.817	75	17.071	-27	.650	-70	6.745	80
8500.000	16.835	74	17.171	-26	.659	-64	7.184	81
9000.000	18.314	72	17.890	-30	.683	-58	7.692	82
9500.000	19.527	70	18.636	-31	.726	-57	8.119	82
10000.00	20.272	66	19.075	-30	.709	-55	8.688	83
10500.00	20.893	66	20.640	-35	.678	-51	9.174	82
11000.00	22.076	65	20.831	-35	.669	-46	9.782	82
11500.00	23.084	64	22.400	-40	.589	-48	10.447	81
12000.00	24.631	63	23.567	-41	.434	-39	11.007	80
12500.00	26.188	61	23.481	-43	.285	-13	11.397	80
13000.00	27.825	60	26.325	-48	.304	52	12.029	82
13500.00	29.952	58	24.729	-49	.713	94	13.496	84
14000.00	33.266	54	24.747	-55	2.167	106	16.547	82

REF PLANE EXT(CM): IN= .00, OUT= .00

PAGE 3: ANA*A5209/DEPT 0810 SEPTEMBER 26,1977
VARIAN METROLOGY LAB/LIONEL WINDHAM
INGAAS DEVICE

.00 VOLTS, .00 MA (MEAS 1) *57-1

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000			1.47	-32.51	.22	3.43
2500.000			1.35	-30.89	.30	2.50
3000.000			1.36	-29.43	.31	2.25
3500.000			1.41	-28.44	.29	2.24
4000.000			1.39	-27.64	.31	1.88
4500.000			1.18	-27.06	.44	1.32
5000.000		14.71	1.23	-26.61	.53	.94
5500.000		13.81	1.21	-26.31	.59	.77
6000.000		13.59	1.29	-26.00	.57	.74
6500.000		12.85	1.14	-25.79	.63	.64
7000.000	12.23	11.41	.81	-27.55	1.10	.37
7500.000	13.12	10.99	.84	-27.97	1.04	.31
8000.000	13.21	10.74	.51	-27.88	1.03	.30
8500.000		10.78	.27	-28.05	.91	.31
9000.000	13.44	10.20	.18	-28.26	1.01	.26
9500.000	12.71	9.91	.02	-28.16	1.05	.24
10000.00	11.57	9.51	-.16	-28.76	1.20	.20
10500.00	11.05	9.48	.23	-29.43	1.40	.17
11000.00	9.76	8.58	-.15	-30.01	1.80	.13
11500.00	9.03	8.30	.06	-31.53	2.48	.10
12000.00	8.20	7.75	-.01	-34.71	4.17	.06
12500.00	7.57	7.26	-.46	-38.77	7.24	.03
13000.00	9.88	9.49	.27	-38.48	4.51	.06
13500.00	10.69	10.26	-.84	-31.64	1.65	.17
14000.00		8.57	-2.16	-23.31	.96	.34

REF PLANE EXT(CM): IN= .00, OUT= .00

Run
#57-2

PAGE 2: ANA#A5209/DEPT 0810 SEPTEMBER 26,1977
VARIAN METROLOGY LAB/LIONEL WINDHAM
INGAAS DEVICE

.00 VOLTS, .00 MA (MEAS 1) 57-2

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	3.691	86	15.207	-7	.269	-88	1.728	65
2500.000	4.563	85	15.224	-10	.330	-89	2.004	66
3000.000	5.648	84	15.510	-11	.395	-88	2.398	71
3500.000	6.643	85	15.790	-11	.449	-86	2.850	74
4000.000	7.849	84	16.244	-12	.509	-85	3.341	76
4500.000	8.733	82	16.308	-16	.556	-85	3.595	76
5000.000	9.989	81	17.031	-17	.609	-85	4.133	76
5500.000	11.153	80	17.617	-18	.650	-84	4.611	76
6000.000	12.682	79	18.422	-19	.694	-82	5.195	78
6500.000	14.237	79	18.955	-20	.714	-82	5.779	79
7000.000	15.651	77	19.239	-23	.699	-82	6.342	80
7500.000	17.046	75	20.148	-23	.671	-77	6.832	80
8000.000	18.306	73	20.122	-26	.700	-72	7.339	80
8500.000	18.951	71	19.969	-26	.712	-76	7.875	81
9000.000	19.700	69	20.561	-28	.638	-52	8.169	80
9500.000	20.184	71	21.309	-29	.781	-60	8.713	81
10000.00	21.906	71	21.652	-28	.679	-61	9.337	81
10500.00	23.852	70	23.562	-32	.635	-54	9.767	79
11000.00	25.663	68	24.065	-32	.623	-50	9.954	79
11500.00	26.973	66	25.911	-37	.528	-50	10.457	80
12000.00	28.736	65	27.117	-37	.378	-42	11.051	82
12500.00	30.320	63	26.748	-39	.206	-11	11.779	83
13000.00	32.218	63	29.869	-43	.307	76	12.880	85
13500.00	34.550	61	27.675	-44	1.001	101	14.760	86
14000.00	41.378	56	26.045	-43	4.185	78	19.769	73

REF PLANE EXT(CM): IN= .00, OUT= .00

PAGE 3: ANA#A5209/DEPT 0810 SEPTEMBER 26,1977
VARIAN METROLOGY LAB/LIONEL WINDHAM
INGAAS DEVICE

.00 VOLTS, .00 MA (MEAS 1) 57-2

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000			3.02	-32.03	.18	4.03
2500.000			2.84	-30.44	.28	2.68
3000.000			2.81	-29.06	.29	2.34
3500.000			2.80	-28.12	.26	2.43
4000.000			2.74	-27.35	.29	1.84
4500.000			2.47	-26.88	.43	1.26
5000.000		15.13	2.42	-26.51	.53	.90
5500.000		14.26	2.34	-26.32	.58	.73
6000.000		13.89	2.31	-26.17	.59	.68
6500.000		13.25	2.10	-26.38	.66	.57
7000.000		12.28	1.74	-27.06	.85	.42
7500.000		11.61	1.63	-27.92	.98	.32
8000.000	12.74	10.76	1.15	-28.02	1.09	.27
8500.000	11.16	10.02	.79	-28.17	1.31	.22
9000.000	11.72	9.90	.72	-29.45	1.31	.18
9500.000	12.48	10.06	.89	-27.83	1.10	.23
10000.00	11.10	9.72	.58	-29.49	1.44	.18
10500.00	10.10	9.12	.68	-30.71	1.95	.13
11000.00	9.34	8.49	.35	-31.40	2.36	.11
11500.00	9.70	9.02	.63	-33.19	2.73	.09
12000.00	10.02	9.45	.61	-36.51	3.65	.07
12500.00	10.31	9.98	.14	-42.15	6.10	.04
13000.00	12.85	12.43	.68	-39.09	2.63	.11
13500.00		12.97	-.69	-29.53	.83	.45
14000.00	3.43	3.26	-4.13	-20.01	1.59	.18

REF PLANE EXT(CM): IN= .00, OUT= .00

10897WATS
21 NOVEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 58-3 V_0 V_c=0 Run #58-3
BIAS= 2.50 VOLTS,

Y REAL AND IMAGINARY

FREQ	11		21		12		22	
2000.00	.09	3.19	12.92	-1.74	.00	-.12	.86	1.98
2500.00	.30	3.92	16.22	-1.16	.02	-.15	.89	2.30
3000.00	.50	4.79	15.95	-1.76	.02	-.19	.82	2.70
3500.00	.57	5.48	15.66	-4.42	.02	-.21	.81	3.08
4000.00	.66	6.34	16.62	-1.05	.03	-.18	.87	3.57
4500.00	.84	7.30	16.28	-4.55	.07	-.23	.93	4.13
5000.00	.96	8.45	15.61	-3.02	.09	-.22	1.01	4.62
5500.00	1.34	9.25	16.75	-3.40	.16	-.22	1.00	5.13
6000.00	1.54	10.34	18.12	-4.20	.19	-.30	.97	5.78
6500.00	1.97	11.53	15.28	-5.70	.13	-.25	1.08	6.81
7000.00	2.21	12.73	18.59	-7.74	.14	-.27	1.20	7.28
7500.00	2.67	14.20	16.72	-4.48	.16	-.21	1.43	7.92
8000.00	3.00	15.20	18.37	-9.02	.14	-.14	1.54	8.48
8500.00	3.46	16.31	20.03	-5.65	.19	-.07	1.67	8.80
9000.00	4.02	17.19	19.94	-8.11	.11	-.00	1.70	9.42
9500.00	4.98	17.62	17.47	-8.09	.16	.22	1.67	9.48
10000.00	5.80	18.06	17.09	-7.34	.15	.41	1.79	10.09
10500.00	5.86	19.31	23.12	-6.03	.38	.71	2.30	10.95
11000.00	7.09	20.97	24.75	-10.22	.64	.71	2.36	10.78
11500.00	8.61	22.53	23.16	-12.14	.70	.75	1.24	11.84
12000.00	11.80	23.50	19.81	-12.17	.50	.86	1.87	13.67
12500.00	12.58	22.31	19.94	-10.00	.57	1.47	2.64	14.25
13000.00	13.55	25.37	29.16	-8.64	.92	2.59	4.06	16.28
13500.00	14.55	23.41	33.25	-23.19	2.12	.35	4.48	10.41
14000.00	12.70	25.09	23.34	-21.59	.88	.98	2.30	13.47

10897WATS
21 NOVEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 58-3
BIAS= 2.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	1.8	.17	26.8	17.0	9.6	305.5	8.0	180.1	419.5
2500.00	3.5	.13	24.0	12.5	18.3	246.5	7.9	133.6	364.5
3000.00	3.2	.24	21.7	10.3	20.9	200.4	8.2	95.8	323.0
3500.00	3.2	.46	20.9	9.6	19.4	175.2	8.0	78.3	288.3
4000.00	3.3	.27	20.7	9.5	15.6	152.9	8.0	61.1	255.1
4500.00	3.1	.37	19.2	8.4	15.6	132.0	7.6	50.9	221.1
5000.00	2.3	.28	18.2	8.3	12.5	114.5	7.5	43.2	199.4
5500.00	2.7	.15	17.7	7.2	14.0	103.7	7.8	33.3	181.4
6000.00	3.1	.13	17.7	6.8	13.0	92.0	7.8	26.4	160.7
6500.00	1.4	.77	14.7	5.9	14.2	82.8	7.4	22.8	139.6
7000.00	2.9	.78	15.4	5.6	13.0	74.7	6.9	22.4	129.7
7500.00	1.1	1.32	14.8		6.2	63.3		4.7	114.6
8000.00	1.5	1.91	14.4		7.7	60.5		11.3	109.2
8500.00	1.9	1.90	14.6		5.9	57.9		12.9	107.6
9000.00	1.8	5.01	13.1		10.8	55.2		14.2	102.7
9500.00	.6	2.29	12.2		11.5	56.9		12.6	106.6
10000.00	-.0	1.88	10.9		12.4	58.3		12.2	102.5
10500.00	1.7	.72	11.9	3.8	13.2	49.0	6.3	14.2	90.0
11000.00	2.2	.40	12.4	3.6	12.7	44.1	6.6	13.3	89.6
11500.00	1.6	-.14	16.0	3.3	13.2	39.7	11.1	3.8	82.6
12000.00	-.6	.99	9.8	2.4	16.2	35.0	8.0	6.7	72.1
12500.00	-1.2	1.14	9.2		11.0	53.7		4.9	74.8
13000.00	.5	.73	9.4	2.5	15.3	34.3	6.3	8.6	62.5
13500.00	3.4	.59	9.8	2.4	15.0	31.5	4.1	21.3	76.1
14000.00	1.6	.40	11.8	2.6	14.2	32.6	7.6	7.3	70.5

10897WATS
21 NOVEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET V_O
SER# 58-6 2VOLTS
BIAS= ~~2.50 VOLTS~~ Run #58-6

Y REAL AND IMAGINARY!

FREQ	11		21		12		22	
2000.00	.10	3.45	15.52	-2.74	.00	6.12	1.95	1.53
2500.00	.29	4.20	18.87	-3.41	.05	-.11	1.18	3.36
3000.00	.49	5.07	18.41	-3.47	.04	-.18	2.05	3.23
3500.00	.55	5.77	18.41	-6.55	.04	-.16	1.28	3.66
4000.00	.58	6.66	19.00	-2.51	.06	-.16	1.91	4.11
4500.00	.75	7.57	18.12	-6.28	.07	-.16	1.44	4.69
5000.00	.76	8.75	17.75	-4.55	.11	-.16	2.23	5.67
5500.00	1.04	9.44	18.28	-5.90	.22	-.17	3.97	5.46
6000.00	1.13	10.77	18.62	-5.41	.08	-.21	2.39	4.75
6500.00	1.59	11.89	16.19	-6.67	.10	-.10	2.04	6.00
7000.00	1.87	13.08	20.00	-8.66	.18	-.05	1.76	6.83
7500.00	2.26	14.50	17.94	-5.29	.18	.01	1.83	7.60
8000.00	2.67	15.53	19.56	-5.77	.18	.13	1.94	8.05
8500.00	3.20	16.62	21.41	-6.41	.30	.20	2.14	8.56
9000.00	3.55	17.37	21.94	-9.45	.27	.29	1.94	9.17
9500.00	4.29	18.37	18.69	-9.02	.37	.37	2.02	9.28
10000.00	5.41	19.06	18.87	-8.25	.37	.52	2.15	9.87
10500.00	5.65	20.28	25.09	-7.22	.40	.78	2.48	11.02
11000.00	6.47	22.00	26.41	-11.41	.31	.83	2.97	10.50
11500.00	7.94	23.66	24.66	-13.11	.56	1.30	1.42	11.59
12000.00	10.12	24.75	21.50	-11.67	.51	1.32	2.16	14.48
12500.00	10.52	25.28	22.12	-9.39	.12	2.55	1.46	15.02
13000.00	11.80	28.25	31.12	-8.56	.39	3.06	2.95	15.98
13500.00	12.75	30.22	39.25	-23.31	1.06	3.33	4.33	13.56
14000.00	11.66	34.12	26.06	-20.72	.31	3.95	2.28	17.69

10897WATS
21 NOVEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET
SER# 58-6 2VOLTS
BIAS= 2.50 VOLTS, .00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	2.9	.38	24.3	16.4	9.6	283.2	4.9	303.1	248.6
2500.00	4.8	.04	24.6	13.0	14.7	231.2	6.9	87.2	258.6
3000.00	4.0	.51	19.3	10.5	18.0	189.5	4.8	131.6	214.8
3500.00	4.6	.53	20.9	9.9	16.6	167.4	6.5	81.9	234.4
4000.00	4.0	.47	19.3	10.1	12.2	145.9	5.1	87.9	195.3
4500.00	4.0	.55	19.2	9.1	12.6	128.3	6.2	57.4	189.5
5000.00	3.0	.62	17.0	9.3	9.5	111.7	4.7	57.8	149.8
5500.00	2.7	.93	14.0	8.5	10.0	102.7	2.8	81.9	118.9
6000.00	3.1	1.12	17.2		1.8	85.5		19.0	145.3
6500.00	1.9	2.23	14.7		7.9	79.5		27.1	143.9
7000.00	3.5	.82	15.9	6.6	10.0	74.3	5.8	33.1	135.2
7500.00	1.7	1.48	16.1		1.8	68.0		12.4	127.5
8000.00	2.1	1.37	16.1		2.9	65.6		14.5	127.1
8500.00	2.5	.75	13.6	5.4	10.0	58.3	5.7	23.9	110.4
9000.00	2.9	.51	14.4	5.2	10.1	55.8	6.3	18.5	104.9
9500.00	1.2	.65	12.1	4.7	10.9	52.1	6.2	18.5	103.3
10000.00	.7	.91	10.9	4.0	12.7	49.5	6.1	17.1	97.9
10500.00	2.4	.53	12.8	4.2	11.3	47.5	6.2	14.6	89.6
11000.00	2.7	.79	12.0	4.0	11.1	43.4	5.3	19.7	91.9
11500.00	2.3	-.21	19.2	3.9	10.8	39.9	13.1	2.5	85.8
12000.00	-.2	.51	11.0	3.1	12.9	36.0	8.1	6.1	68.6
12500.00	-.1	.06	26.7	3.1	13.0	37.0	23.7	.2	69.7
13000.00	1.5	.32	14.7	3.3	11.5	34.2	9.9	3.8	66.6
13500.00	4.4	-.06	19.0	4.4	8.1	32.6	10.2	4.0	73.3
14000.00	.7	-.28		5.1	6.1	28.7		-1.7	56.5

10897WATS
21 NOVEMBER 1977

VARIAN ASSOCIATES TEST REPORT V_d=2V V_g=0V
CENTRAL RESEARCH FET
SER# 59-1 2VOLTS V_G
BIAS= 2.50 VOLTS; Run #59-1

Y REAL AND IMAGINARY!

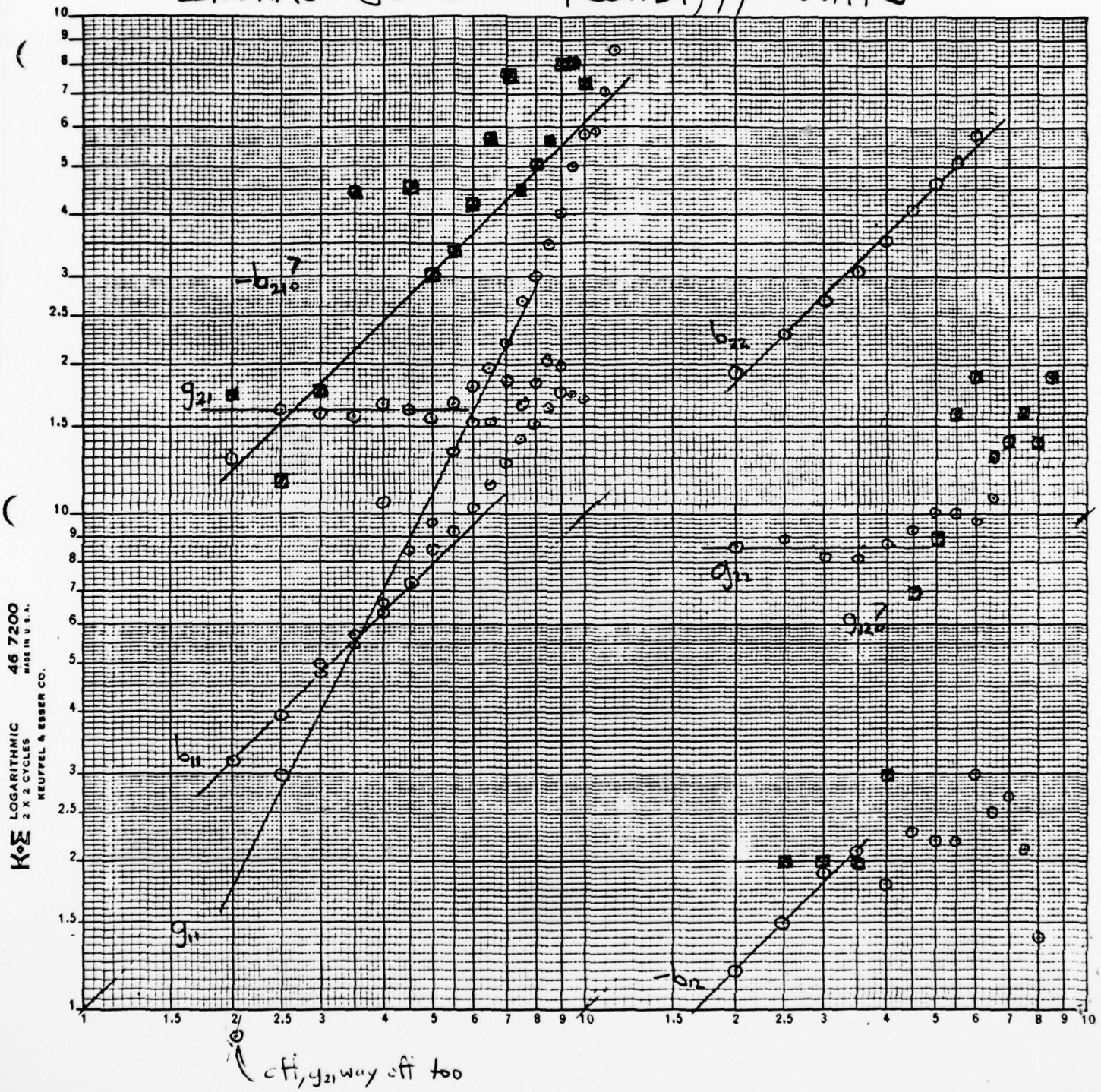
FREQ	11		21		12		22	
2000.00	.01	3.13	14.69	-1.91	.01	-.15	2.03	2.03
2500.00	.21	3.79	18.00	-1.45	.02	-.18	2.13	2.45
3000.00	.35	4.51	17.94	-2.29	.03	-.24	2.13	2.93
3500.00	.38	5.18	17.62	-4.89	.02	-.26	2.18	3.32
4000.00	.44	5.99	18.53	-1.59	.03	-.24	2.33	3.77
4500.00	.58	6.87	17.97	-5.05	.06	-.30	2.49	4.24
5000.00	.60	7.94	17.50	-3.63	.07	-.32	2.69	4.72
5500.00	.86	8.62	18.59	-4.03	.11	-.32	2.80	5.21
6000.00	.83	9.69	19.97	-4.81	.12	-.35	2.88	5.99
6500.00	1.26	10.75	17.34	-6.21	.12	-.27	3.14	7.12
7000.00	1.41	11.83	20.50	-8.14	.16	-.31	3.25	7.77
7500.00	1.87	13.02	19.00	-5.12	.21	-.26	3.54	8.53
8000.00	2.16	13.91	20.44	-5.37	.23	-.21	3.34	9.38
8500.00	2.52	14.81	21.81	-5.96	.30	-.16	3.34	9.72
9000.00	2.66	15.72	21.62	-8.25	.27	-.16	3.36	10.34
9500.00	3.06	16.69	19.25	-8.19	.25	-.03	3.33	9.96
10000.00	3.85	18.06	19.09	-7.43	.38	.15	3.20	10.53
10500.00	4.80	19.03	24.53	-6.72	.44	.21	3.96	11.36
11000.00	5.52	19.72	26.25	-9.95	.52	.45	4.40	11.68
11500.00	5.64	20.28	26.03	-10.56	.87	.54	3.89	13.55
12000.00	6.16	21.81	25.94	-10.14	.63	.43	5.83	17.03
12500.00	6.76	23.97	30.00	-11.19	.90	1.25	9.41	16.50
13000.00	10.56	26.37	37.25	-17.91	1.52	1.71	14.28	20.37
13500.00	11.95	25.22	35.87	-21.31	2.29	.36	16.41	8.47
14000.00	11.34	25.22	32.44	-23.00	1.44	.52	8.17	8.50

10897WATS
21 NOVEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET
SER# 59-1 2VOLTS
BIAS= 2.50 VOLTS; .00 MA

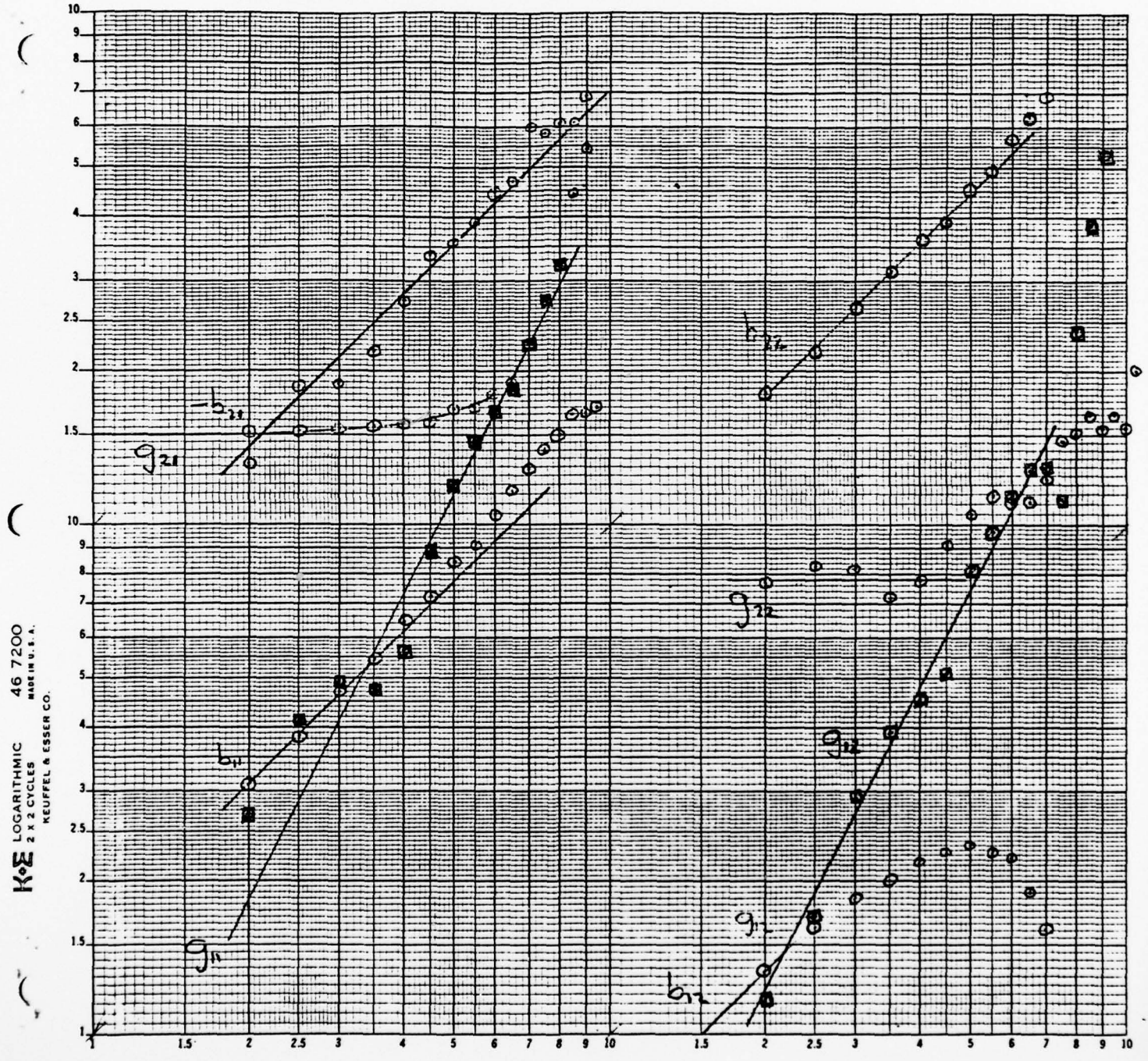
FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000.00	2.4	.08	31.0	23.9	2.0	309.8	4.7	234.4	243.8
2500.00	3.9	.20	22.5	13.9	14.0	253.1	4.6	187.9	228.5
3000.00	3.8	.39	20.0	11.6	17.2	211.3	4.6	149.8	215.6
3500.00	3.8	.56	19.1	10.9	15.7	184.8	4.5	129.9	200.4
4000.00	3.7	.43	18.9	10.9	12.1	160.7	4.3	111.3	185.7
4500.00	3.5	.58	17.3	9.7	12.6	139.5	4.1	96.8	167.6
5000.00	2.9	.53	16.6	9.9	9.5	121.5	3.9	85.9	153.5
5500.00	3.1	.60	15.6	8.7	11.0	111.5	3.8	74.8	143.2
6000.00	3.5	.56	16.0	8.8	8.9	99.3	3.7	61.9	129.7
6500.00	2.1	1.37	14.3		6.1	85.7		21.7	102.5
7000.00	3.3	1.09	16.2		1.4	77.0		14.0	93.5
7500.00	1.8	1.58	13.2		6.1	71.5		21.0	93.8
8000.00	2.2	1.62	13.7		5.8	67.4		17.9	90.5
8500.00	2.4	1.42	14.3		4.9	63.7		12.6	90.8
9000.00	2.4	1.80	13.4		6.8	59.7		15.0	86.2
9500.00	1.3	3.00	11.5		8.0	57.5		20.0	91.5
10000.00	.7	1.94	11.4		6.9	54.6		15.2	92.6
10500.00	1.9	2.11	11.2		8.0	52.1		18.2	85.9
11000.00	2.3	1.56	11.7		7.3	51.6		16.5	87.1
11500.00	2.1	.54	11.2	4.4	10.4	46.0	4.7	15.2	68.2
12000.00	.6	2.37	9.1		8.3	45.3		12.6	57.4
12500.00	.5	1.75	8.2		7.1	43.3		17.6	55.2
13000.00	.6	2.26	6.2		10.0	37.2		21.2	43.3
13500.00	.5	3.60	4.1		11.8	34.1		47.4	33.5
14000.00	2.7	2.06	8.3		9.3	35.7		44.9	84.8

INGAAS 58-3 Nov. 21, '77 WATS



$V_D = 2.5V$ $V_G = 0$

InGaAs 58-3 Oct. 26, 77 Bldg IC Varian



$V_D = 2.5V$ $V_G = 0$

1000WATS
6 DECEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 61-1 2 ✓ Vg = 0
BIAS= ,00 VOLTS.

Run #61-1

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000,00	,10	2,85	16,16	-1,70	,01	-,11	1,00	2,36
2500,00	,17	3,38	16,50	-2,36	,02	-,14	1,20	2,70
3000,00	,25	4,10	16,50	-2,77	,03	-,16	1,35	3,15
3500,00	,46	4,70	16,81	-3,38	,03	-,18	1,51	3,59
4000,00	,44	5,37	16,59	-3,50	,05	-,18	1,53	4,11
4500,00	,52	6,20	16,53	-4,43	,06	-,19	1,64	4,83
5000,00	,57	7,02	17,28	-4,70	,09	-,20	1,76	5,65
5500,00	,60	7,75	17,12	-5,29	,09	-,20	1,96	6,68
6000,00	,73	8,67	18,06	-5,69	,12	-,18	3,48	8,17
6500,00	1,03	9,48	16,97	-7,98	,13	-,18	3,84	9,55
7000,00	1,14	10,41	16,28	-8,64	,12	-,15	3,30	7,15
7500,00	1,57	11,27	17,44	-7,35	,18	-,00	2,98	6,63
8000,00	1,80	11,91	17,56	-7,73	,29	,01	2,61	7,48
8500,00	2,00	12,59	17,59	-8,05	,33	-,09	2,58	7,99
9000,00	2,24	13,42	17,28	-8,81	,27	,03	2,36	8,67
9500,00	2,61	14,30	17,34	-8,77	,28	,14	2,47	9,31
10000,00	2,96	15,42	17,87	-9,59	,29	,30	2,51	10,09
10500,00	3,25	16,44	18,06	-10,73	,39	,42	2,65	10,62
11000,00	3,37	17,22	17,91	-10,97	,41	,55	2,46	10,89
11500,00	3,99	18,37	18,31	-12,14	,48	,73	2,48	11,69
12000,00	4,51	19,19	17,94	-13,09	,56	,96	2,57	12,25
12500,00	5,16	20,34	18,53	-13,84	,64	1,33	2,49	13,00
13000,00	6,53	21,78	16,03	-14,16	1,21	2,17	3,11	14,18
13500,00	10,05	20,81	21,62	-17,50	3,58	,60	5,61	12,34
14000,00	8,75	21,03	19,25	-19,81	1,66	,13	3,44	11,75

1000WATS
6 DECEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 61-1 2
BIAS= ,00 VOLTS, ,00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000,00	3,6	,13	27,9	16,9	12,3	341,4	7,4	144,3	350,4
2500,00	3,7	,16	25,1	14,7	14,6	285,9	6,8	128,9	300,0
3000,00	3,5	,27	22,8	12,9	15,3	235,5	6,3	108,6	259,0
3500,00	3,5	,47	20,0	10,6	20,4	204,7	5,9	94,7	228,9
4000,00	3,3	,35	20,1	10,9	15,0	180,5	5,9	75,9	207,4
4500,00	3,2	,44	19,1	10,3	13,3	156,2	5,7	60,4	180,5
5000,00	3,3	,35	18,9	10,1	11,2	136,1	5,5	48,1	157,0
5500,00	3,0	,41	18,3	10,0	9,7	125,4	5,2	38,9	134,6
6000,00	2,6	,97	15,4	9,3	9,5	112,3	3,5	42,7	102,0
6500,00	2,4	1,66	14,4		4,9	99,4		43,3	114,8
7000,00	1,7	1,98	14,0		7,4	91,4		32,2	107,6
7500,00	2,3	1,78	15,1		5,4	86,6		28,0	135,5
8000,00	2,3	,79	13,6	6,8	11,0	81,5	4,6	38,2	118,6
8500,00	2,2	,70	13,3	6,4	11,0	76,5	4,8	32,7	112,9
9000,00	1,9	1,08	16,9		,0	72,3		4,9	110,0
9500,00	1,6	1,13	15,8		,1	69,8		9,6	106,4
10000,00	1,6	,77	12,3	5,6	10,5	63,0	5,3	20,3	93,9
10500,00	1,5	,47	12,4	5,5	9,9	58,9	5,3	18,6	89,0
11000,00	1,4	,20	12,9	5,6	9,2	56,5	5,9	15,7	86,0
11500,00	1,4	,10	12,9	5,3	9,2	52,6	6,2	12,9	82,5
12000,00	1,1	,01	12,7	5,1	9,2	50,2	6,4	11,4	78,7
12500,00	1,1	-,14	13,3	5,1	8,9	47,4	7,4	8,3	74,9
13000,00	,2	-,20	12,5	4,8	8,8	43,5	7,5	7,0	67,7
13500,00	,6	,24	7,5	3,2	12,7	37,8	3,7	18,3	62,0
14000,00	1,4	,56	8,9	3,0	14,0	39,2	4,5	17,7	72,7

10909WATS
6 DECEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 61-2,2V $V_g = 0V$
BIAS= ,00 VOLTS, Run #61-2

Y REAL AND IMAGINARY:

FREQ	11		21		12		22	
2000,00	,10	3,09	18,59	-1,80	,01	-,09	,07	2,16
2500,00	,20	3,68	19,00	-2,18	,02	-,11	,20	2,33
3000,00	,29	4,48	18,91	-2,75	,02	-,13	,21	2,75
3500,00	,48	5,13	18,97	-3,34	,03	-,14	,49	3,05
4000,00	,47	5,85	18,72	-3,65	,04	-,14	,35	3,44
4500,00	,56	6,75	18,66	-4,45	,05	-,15	,38	4,00
5000,00	,65	7,67	19,31	-4,53	,07	-,14	,42	4,54
5500,00	,69	8,48	19,16	-5,16	,09	-,12	,52	5,03
6000,00	,90	9,45	19,50	-5,78	,10	-,11	,66	5,54
6500,00	1,21	10,42	19,44	-6,11	,12	-,08	,83	6,00
7000,00	1,63	11,39	19,91	-6,92	,14	-,04	,80	6,46
7500,00	1,97	12,06	19,62	-7,00	,16	,01	1,00	6,98
8000,00	2,25	12,86	19,84	-7,45	,17	,07	1,22	7,26
8500,00	2,52	13,64	19,84	-7,39	,19	,17	1,33	7,56
9000,00	2,89	14,55	19,56	-8,62	,29	,32	1,53	7,73
9500,00	3,60	15,48	20,06	-8,61	,40	,36	1,73	8,08
10000,00	4,16	16,34	20,19	-9,39	,39	,37	1,66	8,52
10500,00	4,46	17,06	20,87	-10,34	,42	,57	1,73	8,87
11000,00	4,50	17,81	21,28	-10,62	,50	,69	1,69	9,11
11500,00	4,97	19,03	21,84	-12,14	,54	,85	1,77	9,78
12000,00	5,59	19,91	22,00	-13,16	,61	1,06	1,99	10,17
12500,00	6,23	21,34	22,31	-14,55	,65	1,37	1,76	10,78
13000,00	7,38	22,16	21,69	-15,98	,81	1,73	1,86	11,36
13500,00	8,47	24,47	22,28	-17,56	,83	2,67	1,89	12,41
14000,00	12,61	27,72	23,56	-16,94	3,79	6,55	5,50	17,25

10909WATS
6 DECEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 61-2,2V
BIAS= ,00 VOLTS, ,00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000,00	5,2	-,04	40,5	17,0	10,3	315,2	18,3	15,4	446,1
2500,00	5,3	-,03	33,6	14,3	13,5	262,9	14,0	34,2	406,2
3000,00	5,1	,03	31,1	12,5	14,2	216,4	13,5	27,6	346,5
3500,00	4,9	,17	25,7	10,5	17,7	188,5	10,2	49,6	306,6
4000,00	4,8	,05	26,9	10,7	13,5	166,0	11,5	29,7	277,3
4500,00	4,6	,05	26,0	10,1	11,9	143,9	11,2	23,6	239,5
5000,00	4,7	-,03	25,5	9,7	10,5	127,1	11,0	19,7	212,5
5500,00	4,5	-,09	24,4	9,7	9,1	115,2	10,3	19,5	191,8
6000,00	4,4	-,10	22,6	8,8	9,4	103,3	9,4	20,1	174,0
6500,00	4,0	,05	20,4	7,8	10,5	93,8	8,7	21,2	161,1
7000,00	4,0	,03	20,0	6,9	11,3	85,4	9,1	16,8	150,4
7500,00	3,6	,25	18,0	6,3	12,3	80,5	8,2	18,1	139,1
8000,00	3,4	,36	17,0	6,0	12,1	75,5	7,6	19,7	133,4
8500,00	3,2	,31	16,4	5,7	11,9	71,3	7,5	19,2	128,9
9000,00	2,9	,03	15,8	5,6	11,4	67,1	7,3	19,0	125,6
9500,00	2,6	,08	14,6	5,0	12,3	62,1	7,0	19,2	119,1
10000,00	2,5	,21	14,2	4,5	12,9	58,1	7,2	16,6	113,5
10500,00	2,7	,05	14,7	4,5	12,4	56,2	7,5	14,5	109,6
11000,00	2,7	-,13	15,5	4,8	11,1	54,1	8,1	12,1	107,4
11500,00	2,8	-,18	15,9	4,7	10,4	50,7	8,4	9,9	100,2
12000,00	2,6	-,17	15,4	4,6	10,4	48,3	8,3	9,5	95,9
12500,00	2,6	-,31	18,0	4,6	9,7	45,2	10,8	4,7	91,1
13000,00	2,3	-,34	18,5	4,2	10,3	42,8	12,0	3,3	85,8
13500,00	2,2	-,42	6,8	4,6	8,7	39,5	,0	-1,3	79,3
14000,00	-,2	-,28	17,3	5,3	6,4	33,3	12,3	1,6	53,5

1090 9WAYS
6 DECEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

SER# 61-3,2V $V_g = 0V$
BIAS= ,00 VOLTS,

Run #61-3

Y REAL AND IMAGINARY!

FREQ	11		21		12		22	
2000,00	,09	3,02	15,48	-1,78	,01	-,13	1,46	1,81
2500,00	,16	3,61	14,81	-2,27	,01	-,16	1,51	2,07
3000,00	,26	4,37	15,47	-2,45	,02	-,18	1,58	2,46
3500,00	,44	5,00	15,53	-3,30	,02	-,20	1,72	2,79
4000,00	,43	5,70	15,30	-3,24	,04	-,21	1,71	3,16
4500,00	,51	6,57	15,36	-3,73	,05	-,22	1,74	3,65
5000,00	,53	7,47	15,72	-4,07	,06	-,23	1,72	4,16
5500,00	,58	8,28	15,84	-4,23	,07	-,23	1,70	4,59
6000,00	,79	9,27	16,16	-5,02	,08	-,21	1,77	5,12
6500,00	1,13	10,14	16,59	-5,30	,11	-,19	1,86	5,66
7000,00	1,32	11,11	16,50	-5,91	,13	-,16	1,81	6,09
7500,00	1,74	12,05	16,81	-6,23	,16	-,12	1,96	6,62
8000,00	2,03	12,81	16,87	-6,54	,18	-,07	2,06	7,00
8500,00	2,36	13,73	17,06	-6,73	,18	-,03	2,14	7,32
9000,00	3,06	14,67	17,12	-7,84	,16	,19	2,40	7,59
9500,00	4,05	14,95	16,75	-7,83	,36	,23	2,39	7,94
10000,00	3,68	15,19	17,53	-8,70	,41	,20	2,40	8,56
10500,00	3,55	16,25	17,59	-9,64	,37	,30	2,43	9,00
11000,00	3,40	17,12	17,94	-9,89	,38	,47	2,32	9,33
11500,00	3,81	18,56	17,72	-11,39	,44	,66	2,43	10,05
12000,00	4,52	19,37	18,00	-11,81	,52	,86	2,65	10,53
12500,00	4,70	20,56	18,47	-13,42	,54	1,12	2,48	11,03
13000,00	5,69	21,81	17,59	-14,00	,65	1,52	2,46	11,73
13500,00	6,38	23,66	18,47	-14,44	,70	2,36	2,56	12,78
14000,00	7,95	26,78	18,34	-14,45	2,42	4,57	4,46	15,52

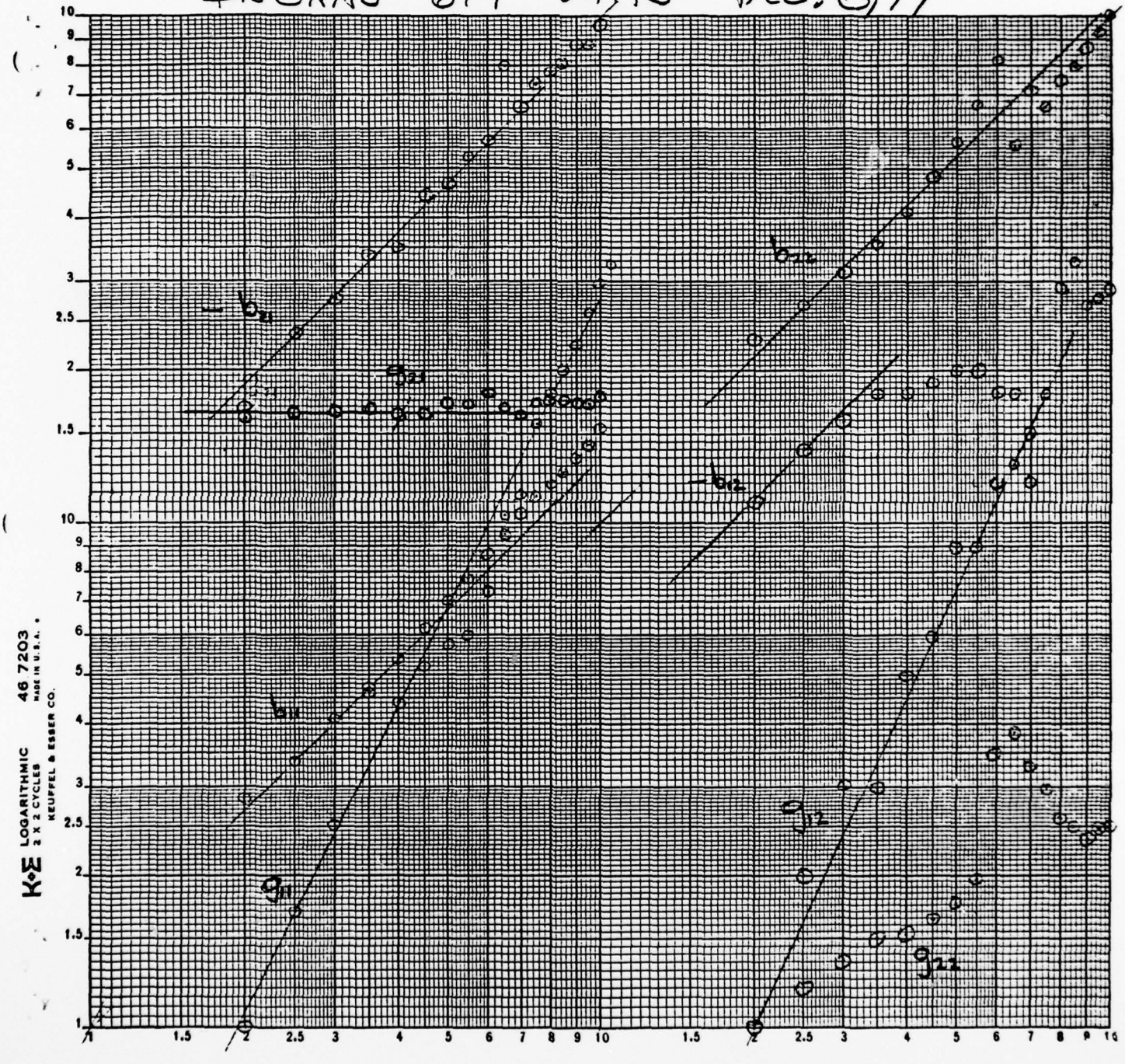
1090 9WAYS
6 DECEMBER 1977

VARIAN ASSOCIATES TEST REPORT
CENTRAL RESEARCH FET

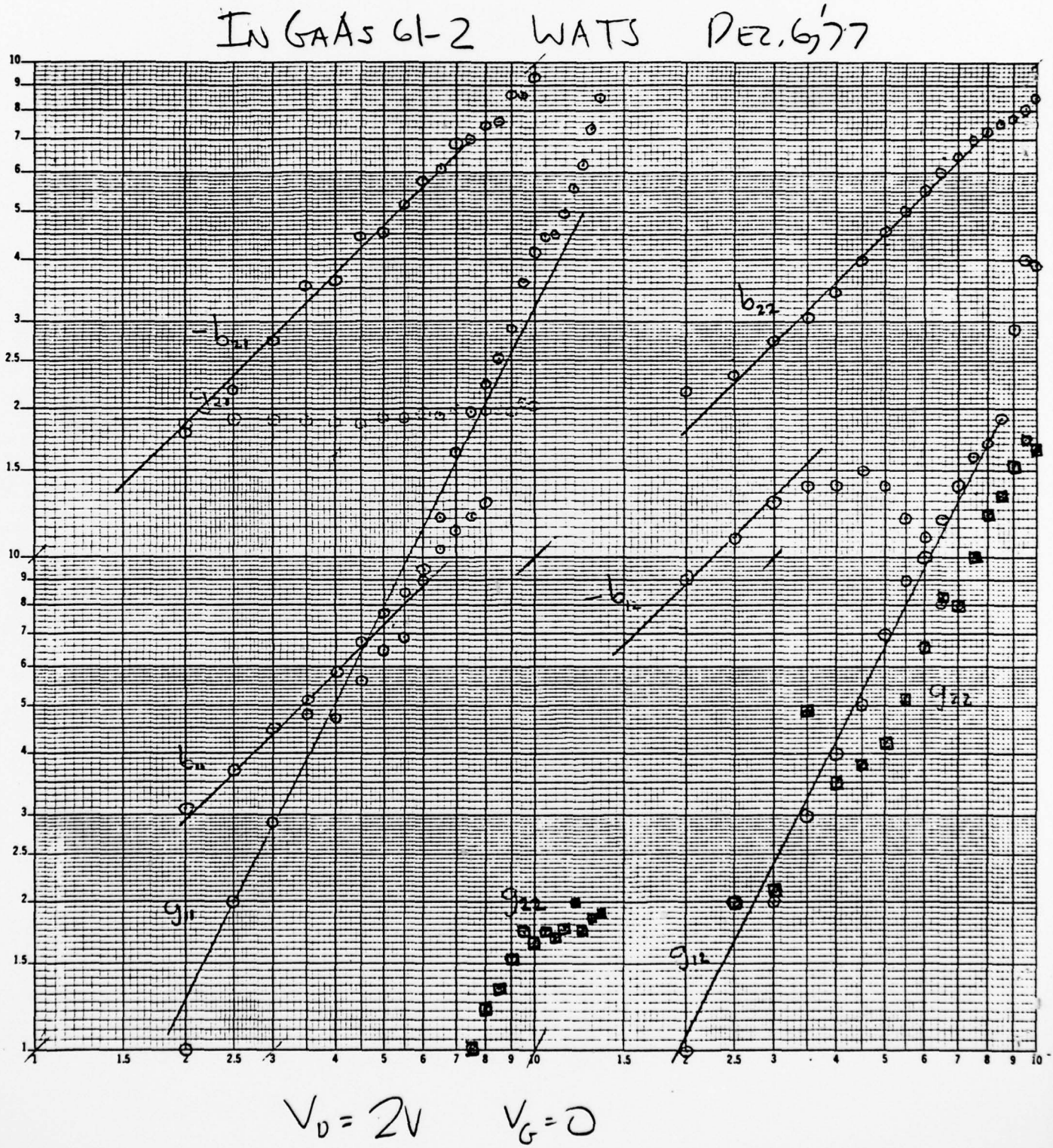
SER# 61-3,2V
BIAS= ,00 VOLTS, ,00 MA

FREQ MHZ	S21 DB	K	GMAX DB	G1 DB	Z MATCH IN R + JX		G2 DB	Z MATCH OUT R + JX	
2000,00	3,1	,19	26,2	17,1	10,5	321,1	6,0	255,5	329,7
2500,00	2,6	,23	23,4	14,9	12,3	268,4	5,8	216,0	307,4
3000,00	2,9	,33	21,4	12,8	14,0	221,9	5,7	171,9	278,9
3500,00	2,8	,57	18,8	10,7	17,7	192,8	5,3	150,6	250,0
4000,00	2,6	,46	18,9	11,0	13,1	169,9	5,4	125,4	236,7
4500,00	2,5	,52	18,2	10,4	11,7	147,7	5,3	101,0	214,8
5000,00	2,6	,44	18,3	10,4	9,4	130,3	5,4	80,9	197,9
5500,00	2,5	,43	18,1	10,1	8,4	117,8	5,5	68,1	185,2
6000,00	2,5	,65	16,9	9,1	9,1	105,3	5,4	58,1	169,1
6500,00	2,4	,91	15,5	7,8	10,6	95,9	5,3	51,1	155,5
7000,00	2,2	,91	15,2	7,5	10,0	87,6	5,5	43,0	147,7
7500,00	2,0	1,36	16,0		6,6	77,5		9,9	133,0
8000,00	1,8	1,63	15,1		4,8	74,3		19,1	129,5
8500,00	1,6	2,06	14,1		5,8	70,2		22,6	126,2
9000,00	1,4	2,19	12,6		9,7	68,8		28,0	131,6
9500,00	,9	1,45	12,4		7,8	67,1		17,5	126,0
10000,00	1,4	,94	11,3	4,7	13,5	62,4	5,2	26,3	108,4
10500,00	1,4	,79	11,7	5,0	11,5	59,2	5,3	24,0	103,9
11000,00	1,5	,33	12,7	5,5	9,6	56,8	5,7	20,6	102,1
11500,00	1,3	,18	12,6	5,5	8,8	52,4	5,9	17,6	94,9
12000,00	1,1	,20	11,9	5,1	9,4	50,0	5,8	16,7	90,5
12500,00	1,3	-,06	13,3	5,4	8,2	47,4	6,6	12,6	87,6
13000,00	,7	-,13	13,0	5,0	8,6	44,3	7,3	9,6	82,5
13500,00	,6	-,25	15,0	5,3	7,4	41,5	9,1	5,6	76,9
14000,00	-1,0	-,33	13,2	6,4	5,0	35,8	7,9	5,5	59,8

InGaAs 61-1 WATS Dec. 6, '77



$V_D = 2V \quad V_G = 0V$


InGaAs 61-2 WATS Dez, 6'77
$-b_{21}$
b_{22}
$-b_{12}$
b_{11}
g_{11}
g_{22}
g_{12}
g_{12}
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